INTEGRATED CIRCUITS

DATA HANDBOOK

ICs for Telecom
ISDN

Philips Semiconductors

PHILIPS

PHILIPS

ICs FOR TELECOM
ISDN

SELECTION GUIDE

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FUNCTIONAL INDEX

NUMERICAL INDEX

GENERAL

Pro electron type designation code for integrated circuits

Basic type number

This type designation applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick- film and hybrid integrated circuits.

A basic type number consists of three letters followed by a serial number.

FIRST AND SECOND LETTER

Digital family circuits

The first two letters identify the family (see note 1).

Solitary circuits

The first letter divides the solitary circuits into:

S : solitary digital circuits
T : analog circuits
U : mixed analog/digital circuits

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 2).

Microprocessors

The first two letters identify microprocessors and correlated circuits as follows:

MA : microcomputer
central processing unit
MB : slice processor (see note 3)
MD : correlated memories
ME : other correlated circuits (interface, clock, peripheral
controller, etc.)

Charge-transfer devices and switched capacitors.

The first two letters identify the following:

NH : hybrid circuits
NL : logic circuits
NM : memories
NS : analog signal processing, using switched capacitors
NT : analog signal processing, using change-transfer
device
NX : imaging devices
NY : other correlated circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range. The letters A to G give information about the temperature:

A : temperature range not specified below (see note 4)
B : 0 to + 70 °C
C : −55 to +125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature rang letter indicating a narrower temperature range may l used or the letter 'A'.

Example : the range 0 to +75 °C can be indicated by 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Prc Electron, or the serial number (which may be a combination of figures and letters) of an existing cor type designation of the manufacturer.

To the basic type number may be added:

Version letter(s)

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack (2 leads)
G : for flat pack (4 leads)
H : for quadrature flat pack (OFP)
L : for chip on tape (foil)
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

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Pro electron type designation code for integrated circuits

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : cylindrical
D : dual-in-line (DIL)
E : power DIL (with external heatsink)
F : flat (leads on 2 sides)
G : flat (leads on 4 sides)
H : quadrature flat pack (QFP)
K : diamond (TO-3 family)
M : multiple-in-line (except dual-, triple-, quadruple-in-line)
Q : quadruple-in-line (QIL)
R : power QIL (with external heatsink)
S : single-in-line
T : triple-in-line
W : lead chip-carrier (LCC)
X : leadless chip-carrier (LLCC)
Y : pin grid array (PGA)

SECOND LETTER: Material

C : metal-ceramic
G : glass-ceramic (cerdip)
M : metal
P : plastic

To avoid confusion when the serial number ends with a letter, a Hyphen is used preceding the suffix.

Examples (see note 5)

PCF1105WP : Digital IC, PC family, operational temperature range −40 to +85 °C, serial number 1105, plastic leaded chip-carrier.

GMB74LS00A-DC: Digital IC, GM family, operational temperature range 0 to +70 °C, company number 74LSS00A, ceramic DIL package.

TDA1000P : Analog circuit, no standard temperature range, serial number 1000, plastic DIL package.

SAC2000 : Solitary digital circuit, operational temperature range −55 to +125 °C.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).

2. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

3. By 'slice processor' is meant: a functional slice of microprocessor.

4. In the case of two same types with two different temperature ranges not specified below, one type should use the letter 'A' as the third letter and the other, the letter 'X'.

5. Some companies have been using version letters and/or two letter-suffix, which differ from the Pro Electron definitions. In case of confusion Pro Electron may be contacted.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.

Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

IST BUS

IST BUS SPECIFICATION

CONTENTS

1.0 INTRODUCTION

The Integrated Services Terminal (IST) bus offers a low
cost in-house communication network. The voice service
and the data service are integrated in one communication
network.

As a stand alone digital communication network the IST
bus provides in-house communication for up to 31 term-
inals within a range of 300 metres. Up to four terminals
can converse simultaneously, while the exchange of data
packets is allowed at the same time.

Interconnection of terminals is via a simple, easy to install,
single twisted-pair cable. Terminals can be connected and
disconnected at any time provided that the total number
connected does not exceed 31. Only administration infor-
mation should be kept on the identification number of
a terminal.

If a wider communication range is required it is possible
to gate data paths via a "gateway" to other networks,
especially a gateway to the ISDN S reference point (note 1).
The 8 kHz synchronous frame of the IST bus could be
synchronized in the gateway to an 8 kHz external source.

The protocol on the IST bus is completely distributed
along the members of the bus. There is no central bus
controller. This ensures a reliable bus system because even
if a terminal fails the communication between others will
not be disturbed.

The IST bus is mainly optimized for voice communication
and offers eight 64 kbit/s circuit-switched channels (b1 to
b8), time multiplexed on an 8 kHz frame structure. The
protocol to access one of these channels is distributed along
the terminals connected on the bus. Each terminal could
access arbitrarily one or more of these circuit-switched
channels. A 64 kbit/s packet-switched data channel (bd)
is provided next to these eight circuit-switched channels.
The bd channel is the IST equivalent of the ISDN "D"
channel. The b1 to b8 channels are the IST equivalent of
the ISDN "B" channels.

Layers 1 and 2 of the 7-layer hierarchy of the Open Sys-
tems Interconnection (OSI) model developed by the Inter-
national Standardization Organization (ISO) built on this
packet-switched channel are specified. Layer 2 offers a
datagram service (note 2) with error free transmission of
data packets and flow control. The access mechanism to
this channel is the slotted CSMA/CD protocol (note 3).
With this protocol access is guaranteed even with a 100%
load. This makes the IST bus also suitable for process control.

The IBI, an IST Bus Interface (PCB2310) is a VLSI circuit
which offers the complete protocols for the b channels and
the protocol up to layer 2 for the data channel. The coup-
ling to the bus will be achieved with a simple transformer.

Notes to the Introduction

1. The ISDN reference point has been specified by the
   CCITT in recommendations I430, I440 and I450.
2. A datagram service is a connectionless service specified
   by ISO; see also section 3.0.
3. CSMA/CD is Carrier Sense Multiple Access with Collision
   Detection. If a collision occurs terminals are allowed
   to transmit only in specific time slots. See bd access
   mechanism.

2.0 LAYER 1 CHARACTERISTICS

2.1 Configuration and definitions

It is possible to connect up to 31 terminals on the IST bus. One or more terminals could have connections to other networks, these terminals are called gateways. A terminal could be any equipment with the facility to communicate digital information to other equipment, e.g.

- digital voice communication : telephone, intercom
- digital data communication : computers, printers, telex, alarm indicators, slow scan television

Physically the interface of the IST bus is a twisted-pair cable leading to all terminals. A digital transmission technique is used for the transfer of data.

Logically the IST bus defines a set of protocols. These protocols specify the distribution of the transmission capability among the connected terminals.

The connection of terminals on the IST bus is limited by the distance between connected terminals being not less than 2 metres. Connection is achieved via a cord with a maximum length of 5 metres and a transformer. Each terminal must have a unique number between 1 and 31.

Because the IST bus is a twisted-pair cable and the voltage on the line is less then 1,25 V, pick-up and emission of radiated interference is minimal.

It is possible to distribute phantom power accross the interface using the same leads that are used for the data transmission due to the fact that the Alternative Mark Inversion (AMI) line code has been used. The voltage must be less than 42,5 V in accordance IEC safety regulations.

A configuration of the IST bus is shown in Fig. 1.

2.2 Input impedance (Z_I)

Because terminals are connected as stubs along the line the input impedance must be such that when 31 terminals are connected digital transmission are not disturbed.

The real part of the impedance should be such that if 31 terminals are located close together the reflections caused by these terminals are less than 10% at 500 kHz.

DC decoupling capacitors should be larger than $1 \mu F$.

2.3 Line characteristics

A twisted pair of cables should be used.
Characteristic impedance must be in the range:

$$Z_O = 75 \text{ to } 150 \, \Omega$$

Correct matching of the line is achieved when the terminating resistance is:

$$R_T = Z_O \pm 2\%$$

The round trip propagation delay must be:

$$T_d \ < 3000 \text{ ns}$$

And the maximum attenuation is:

$$A = 20^{10} \log V_I / V_O < 6 \text{ dB (f = 500 kHz)}$$

2.4 Isolation

The isolation specified here is suitable for in-house systems.

A locally powered terminal must have a security isolation of more then 1500 V.

Terminals should withstand:

- Common mode voltage surge with:
  amplitude = 500 V
  rise time = $1 \mu s$
  fall time = $1000 \mu s$
  The source impedance is $0,015 \mu F$

- Differential mode voltage/current surge with:
  amplitude = 50 V
  rise time = $1 \mu s$
  fall time = $50 \mu s$
  The source impedance has a current limit of 200 mA

DEVELOPMENT DATA
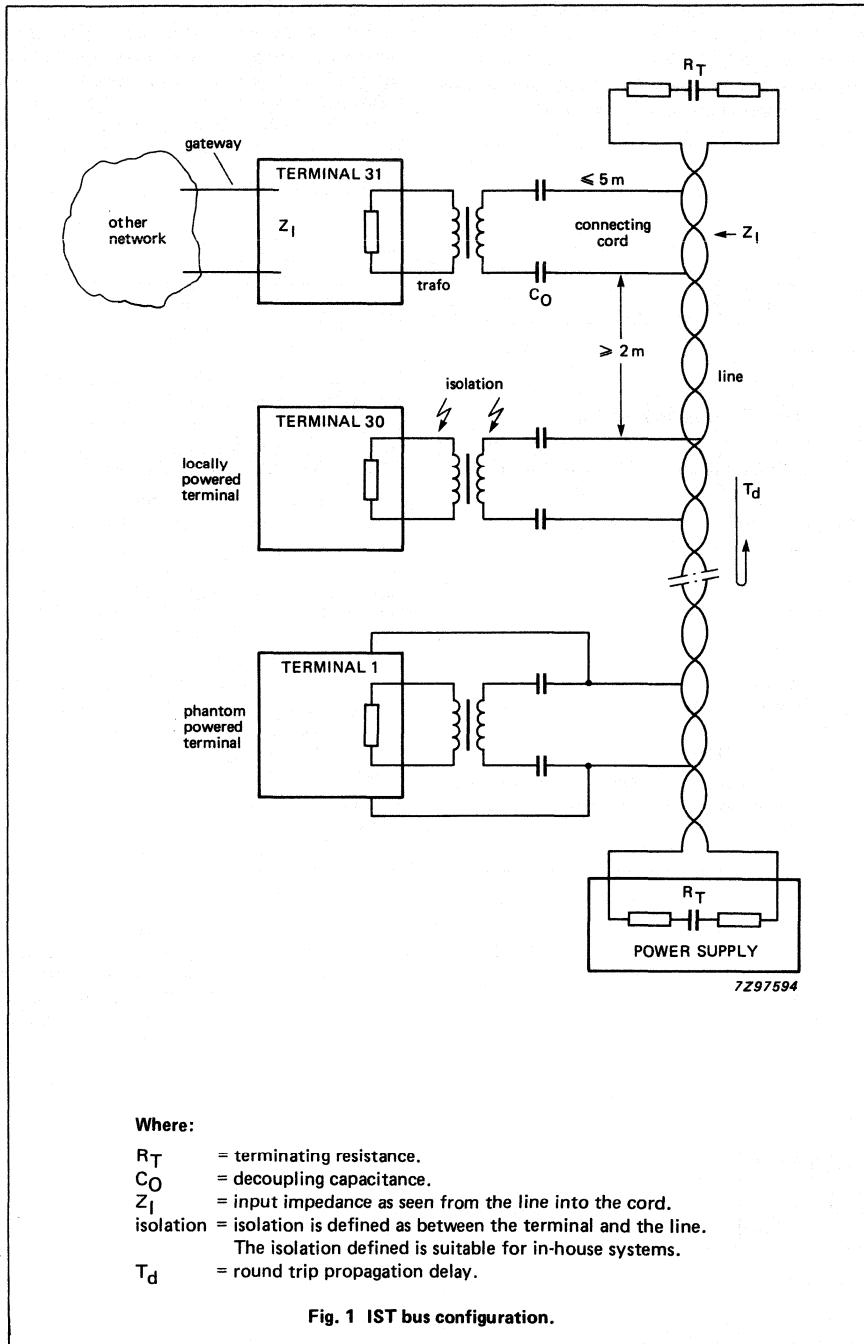
Where:

R_T = terminating resistance.
C_O = decoupling capacitance.
Z_I = input impedance as seen from the line into the cord.
isolation = isolation is defined as between the terminal and the line.
 The isolation defined is suitable for in-house systems.
T_d = round trip propagation delay.

Fig. 1 IST bus configuration.

2.5 Line signal

The line code is Alternative Mark Inversion. A logic 1 will result in a positive or a negative pulse on the line. A logic 0 will result in no signal on the line.

The nominal output voltage will be 1100 mV ± 150 mV into 50 Ω using the test configuration shown in Fig. 2.
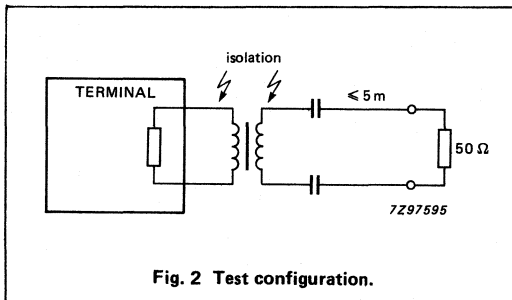
Fig. 2 Test configuration.

The bit rate is 1,024 kbits/s ± 100 ppm; based on an 8,192 kHz ± 100 ppm crystal.

The difference between the positive and the negative pulse should be less than:

$$\int \frac{\text{positive pulse}}{\text{negative pulse}} \, dt < 5\%$$

2.6 Noise immunity

The receiver must have a noise immunity to an input signal of 70 mV rms and below when f = 0 to 1 MHz.

2.7 Receiver input sensitivity

The receiver must handle input pulses as shown by the limits in Fig. 3. This also puts constraints on the transmitter output pulse.
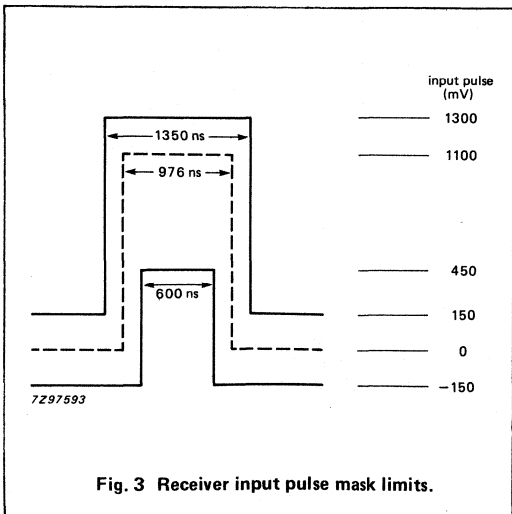
Fig. 3 Receiver input pulse mask limits.

2.8 Phantom power supply

Because the power spectrum of the AMI line code is zero for DC it is possible to distribute phantom power over the signal lines. The power supply of 42,5 V (max.) should not disturb the IST bus. The power available at the terminal is 400 to 600 mW and a maximum of 5 to 10 terminals could be powered. Connecting a terminal to the IST bus could cause the system to go down for some milli seconds.

2.9 Frame structure

A frame of 125 μs ± 122 ns contains ten time division multiplexed channels as shown in Fig. 4:

- 1 x 32 kbit/s synchronization channel ; Frame (F)
- 1 x 64 kbit/s packet-switched channel ; Data (bd)
- 8 x 64 kbit/s circuit-switched channels ; Data/voice (b1 to b8)

Each channel is preceded by an occupied bit which is logic 1 if the channel is occupied (this will result in a positive or a negative line signal). Due to line delays and synchronization a 4 μs shift in the bd and b1 to b8 channels is allowed; 0,5 μs is used as channel separation.

After power up one of the connected terminals should always transmit in the frame channel. The frame signal is coded "0011". The frame channel is used to synchronize all terminals to the 8 kHz frame. The terminal transmitting in the frame channel is the master and the others are the slaves. A fully distributed algorithm called master/slave arbitration determines which terminal will become the master. If a master fails another will automatically take over. One of the terminals connected to another network will always become the master of the IST bus. This terminal could be synchronized with that other network, but this can cause a jitter of 122 ns in the frame. The master/slave procedure is shown in Fig. 7 and Fig. 8.

If a gateway terminal connected to the IST bus is not master it will transmit a broadcast control message called "TOM". The current master will cease transmission in the frame channel as soon as all circuit-switched channels are free and the master/slave procedure restarts.

With a "TRM" primitive a terminal could request frame channel switch-off (after all circuit switched-channels are released) to enable terminal disconnection from the IST bus. A BUS_DOWN, BUS_UP primitive sequence (master) and a BUS_UP primitive (slave) indicates that another terminal is the master of the IST bus.

DEVELOPMENT DATA

Where: 1 bit-period = 8 clock periods

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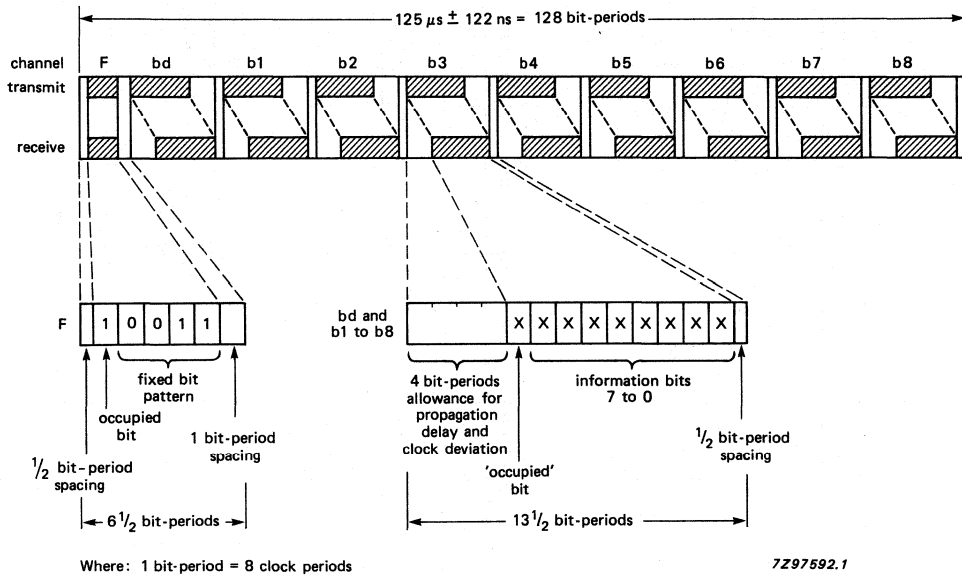
Fig. 4(a) Channel frame structure.
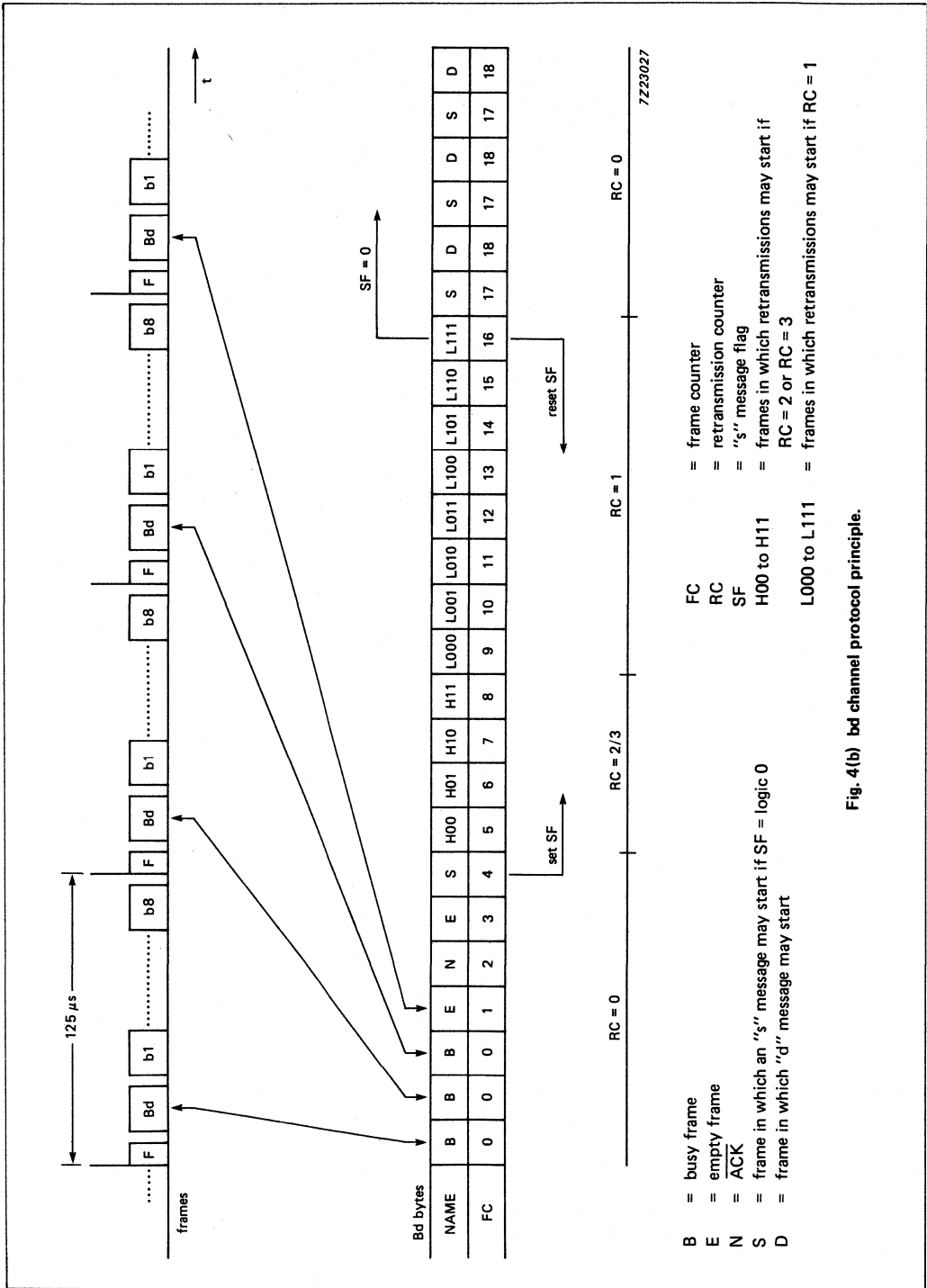
Fig. 4(b) bd channel protocol principle.

B = busy frame
E = empty frame
N = ACK
S = frame in which an "s" message may start if SF = logic 0
D = frame in which "d" message may start

FC = frame counter
RC = retransmission counter
SF = "s" message flag
H00 to H11 = frames in which retransmissions may start if RC = 2 or RC = 3
L000 to L111 = frames in which retransmissions may start if RC = 1

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2.10 Frame alignment

A terminal should recognize the frame signal three consecutive frames before they are synchronized (in-lock). When a synchronized terminal fails to recognize the frame signal for three consecutive frames the terminal is unsynchronized again (out-of-lock). A terminal is only allowed to transmit in one of the bd and/or b1 to b8 channels when synchronized.

2.11 bd access protocol

There are 3 types of message:
- "c" type; control message
- "d" type; data message
- "s" type; signalling message.

Access is determined such that terminals transmitting a "c" type or "s" type message have priority over terminals wanting to transmit "d" type messages. If a terminal has to transmit a "c" and an "s" type message the "c" type has priority. If a collision occurs between messages of the same type, the terminal number is decisive. Collided messages take priority over new messages to guarantee fair access. The terminal number is split into two parts to minimize access times. Table 1 illustrates the priority scheme.

Table 1 Access protocol priority scheme

priority	message	terminal
1	collided "c" or "s"	high number low number
2	new "c" or "s"	—
3	collided "d"	high number low number
4	new "d"	—

To access the bd channel the IST bus uses the CSMA/CD access protocol. The protocol of layer 2 for transmission of "s" and "d" messages is shown in the SDL diagrams, (Figs 9 to 12). The protocol treats "c" messages as "s" messages. In the IBI "s" and "c" messages have priority. The main part of the protocol is the bd channel access system and the frame-counter is closely related to this mechanism. Both of these mechanisms are illustrated in Fig.4(b).

Every IBI includes the frame-counter (FC) which is synchronized at the end of a packet transport in the bd channel whenever the bus is occupied. The frame indicated with B, E, N, S, H00 to H11, L000 to L111 and D have dedicated meanings as shown in Fig.4(b). The end of a packet transport is indicated by a frame in which the bd channel carries no start or information bits, i.e. an EMPTY frame (E). The frame that follows the E frame is the $\overline{ACK}$ (N) frame. In this frame stations may transmit the not acknowledge code, 11111111. This code is used if retransmission is required due to transmission errors, collisions or destination receive buffers full. If the $\overline{ACK}$ code is not needed the frame remains empty.

For circuit implementation reasons the N frame is followed by another E frame. After this first tine messages may access the bd channel in the S frame is SF = logic 0. SF is set to logic 1 if a transport is started in this frame. The 12 frames H00 to H11 and L000 to L111 are intended for retransmission purposes. In this field both signalling and data packets may start if SF = logic 0. If SF = logic 1 only signalling packets may access and data packets must wait for SF = logic 0 to occur.

If the ACK signal appears in the N frame the retransmission counters (RC) of the colliding terminals are increased. Depending on the 3 least significant bits of the 5 bit IST bus terminal address retransmissions will start in frames L000 to L111 when RC = 1. It is still possible that up to 4 stations can collide in this first retransmission period. Stations affected will start a second retransmission in the frames H00 to H11 (RC = 2) depending on the 2 most significant bits of the station's address. During the second retransmission period collisions cannot occur because the involved stations have different address bits.

Reception of $\overline{ACK}$ however is still possible during this second retransmission period, occuring due to noise or inability of the buffer to accommodate the new packet, in order to distinguish between these 2 conditions the transmission is repeated once more in frames H00 to H11 (RC = 3). If after this $\overline{ACK}$ is again received it is concluded that the receiving station was unable to store the packet. The transmitting chip will then warn its controller with a transmission overflow message. With the exception of frame control messages, (which only deal with layer 1), the transmitting chip confirms the transmission of all error free transfers with its controller.

The internal frame-counter is returned to the E position (FC = 3) in frame L111, if SF = logic 1 or access occurs during this frame, in order to give waiting data packets a retransmission chance. SF is reset at this time.

If during frame L111 SF = logic 0 and no access occurs, the internal frame-counters continue with S and D frames sequentially. First time signalling and data packets may start during these frames. This is also the normal access routine when the bd channel has been idle for some time. The S and D frames prevent collision between signalling and data packets.

2.12 b channel access protocol

The b channel access protocol is fully decentralized. All members along the IST bus have the same algorithm. Each terminal is free to occupy any number of b channels provided they are not occupied by another terminal. b channels are not in pairs. To determine which terminal is allowed to access a b channel the access mechanism of the bd channel is used. If a terminal want to access a free b channel, it transmits a unique broadcast control message in the bd channel. This control message is called "OCP". After a successful transfer the terminal is allowed to access the first free b channel. A b channel is **free** if the occupied bit of that channel is logic 0 for at least **two consecutive frames** directly after the control message has been correctly transferred.

The availability of "enquiry or call transfer" is made possible by ordering a terminal to occupy a b channel directly after that specific b channel has been released. A channel is seen **released** if its occupied bit is logic 0 for at least **one frame**.

3.0 LAYER 2 PROTOCOL FOR THE bd CHANNEL

3.1 Service

The service offered by the layer 2 protocol for the bd channel is a packet-switched datagram service. This means it is not necessary to set up a logical link before being able to transfer data packets. Layer 3 data is transferred transparantly by the layer 2 service. Two types of data packets can be transferred:

- "s" type packets for control of circuit-switched channels
- "d" type packets for data packet exchange between terminals

The average transfer delay of "s" types packets is less than that of "d" type packets due to the bd access protocol. The layer 2 message is controlled with a Cyclic Redundancy Check (CRC). If a message is received wrongly it will be retransmitted. Thus an error-free packet transmission can be guaranteed on an erroneous channel. Flow control is possible because a receiver can reject a data packet.

3.2 Protocol

Packets are separated by at least one empty byte. An occupied bit at logic 0 in the bd channel indicates an empty byte. In the packet the occupied bit is set to logic 1 to ensure transparency as shown in Fig. 5.

Each packet will be immediately rejected two frames after the transmission if:

- the calculated CRC in the receiver differs from the received CRC

or

- a receiver is not able to receive the message because of pending messages

If a packet is rejected a not acknowledge ($\overline{ACK}$) will be transferred immediately after the message.

The transmitter will then re-transmit its message in accordance with the bd access protocol. A rejection instead of an acknowledgement has been choosen because broadcast messages can be similarly rejected ("wired NOR"). However, a transmitter cannot detect whether a non-existing or a non-responding terminal has been addressed.
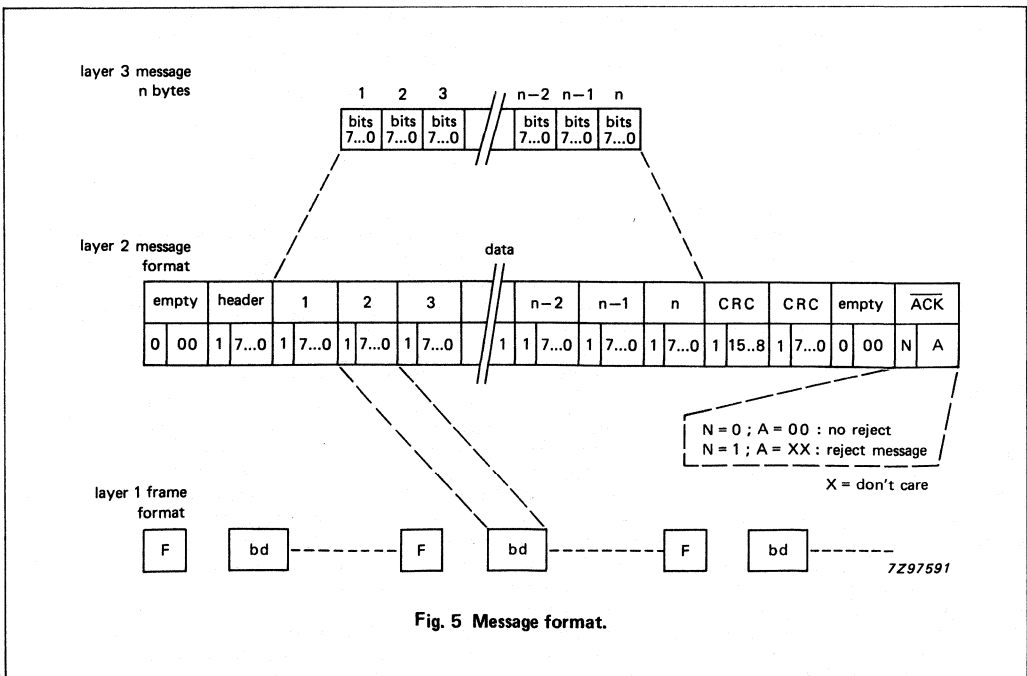
Fig. 5 Message format.

The trailer contains the 16-bit CRC. The CRC operation is a division of the complete layer 2 packet including the header. The divider is:

$$X^{16} + X^{12} + X^5 + 1$$

and the initial remainder is "00".
The final remainder of the division will be transmitted in the two CRC bytes.

The header distinguishes the three types of messages:

- "c" or control type used for control over the frame and b channels
- "d" type which can transfer any kind of data
- "s" signalling type used for routing etc.

The "s" and "d" type messages can address any specified terminal or all terminals (broadcast message). The "c" type messages address all terminals. Table 2 displays an overview of the bits in the header.

3.3 Maintenance

Five control messages are used on the IST bus:

- The "OCP" message is used to control the b channel access and is unique for each terminal because of the terminal number in the header
- The "TOM" message is used to control the frame channel (see master/slave arbitration)
- The "AFS", "SAS" and the "SCO" messages are used to control the external synchronization procedures (see Figs 12 and 13)

If a terminal wants to communicate to another network via a gateway it can ask the IST bus to synchronize with the external 8 kHz source of that network. This procedure is initiated by an EXTERNAL_SYNC_REQUEST (ESR) primitive. If the terminal is not the master on the IST bus it will transmit an "SAS" control message in the bd channel. The gateway terminal will receive an EXTERNAL_SYNC WANTED (ESW) upon receipt of an "SAS" message. If the external synchronization is established the "SCO" control message will be transferred to the bd channel and when received an EXTERNAL_SYNC_IS_ON (ESO) primitive is given.

If the gateway wants to cease the external synchronization it issues an EXTERNAL_SYNC_RELEASE_REQUEST (RES); the "AFS" control message is transferred and all terminals will receive an RELEASE_EXTERNAL_SYNC_PROCEEDS (RSP). If there is no reaction within 8 seconds from other members on the IST bus the master releases the external synchronization.

The following other maintenance services are offered to the layer 3:

- If there is no signal on the IST bus a BUS_DOWN_INDICATION (TMP) primitive is given
- When a signal reappears on the IST bus a BUS_UP INDICATION (TMF) primitive is given
- If the transfer of an "s" or "d" type message is failed an s_FAILURE_INDICATION (FAILURE) or a d_FAILURE INDICATION (FAILURE) is given

A transfer is failed if a reject is still received after 3 retransmissions.

- If a transfer is successful an s_SUCCESS_INDICATION (SUCCESSFUL) or a d_SUCCESS_INDICATION (SUCCESSFUL) primitive is given.

Table 2 Header format

	bit								type	
	7	6	5	4	3	2	1	0		
control messages zero data bits	1	1	X	terminal number(n)					OCP	(occupation of b-channel will proceed)
		0	0	0	0	0	0	1	TOM	(transfer of master request)
				0	0	0	1	0	AFS	(ask/give permission to finish synchronization)
				0	0	0	1	1	SAS	(slave asks for synchronization)
				0	0	1	0	0	SCO	(synchronization is ON)
signalling messages	0	1	X	destination address*					"s"	
data messages	0	0	X	destination address*					"d"	

Where:

X = don't care
* = all zeros indicate the broadcast address

4.0 LAYER 3 OF THE bd CHANNEL

To be specified.

REQUEST RESPONSE

PRIMITIVES

CONFIRMATION INDICATION

LAYER 2 ENTITY

LAYER 2 ENTITY

bd channel IST bus

7Z97596
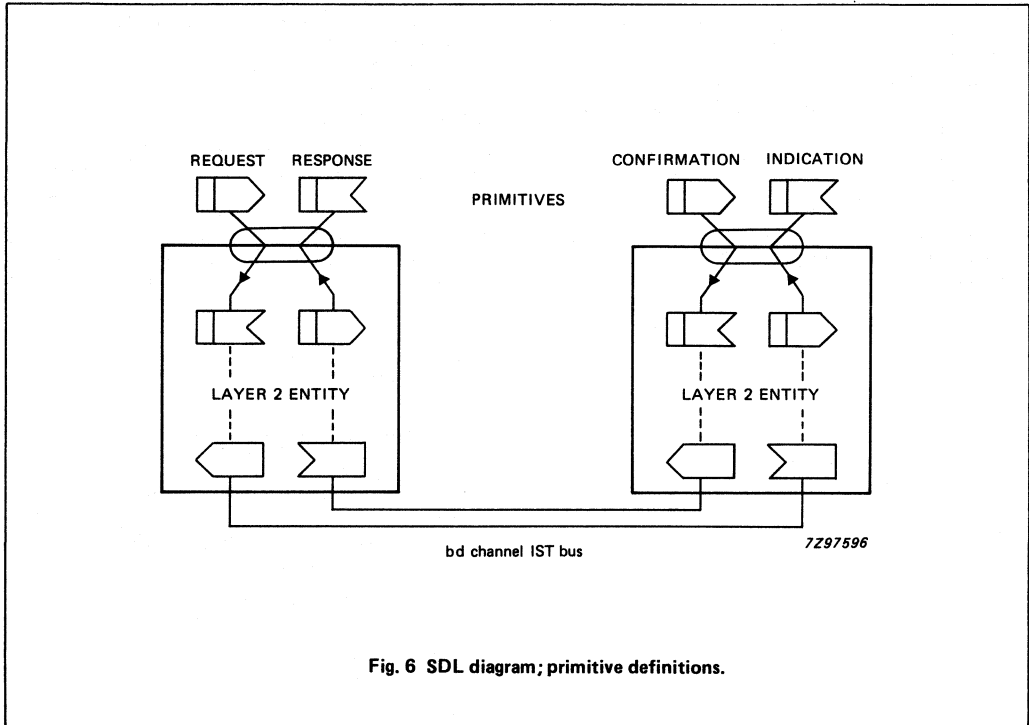
Fig. 6 SDL diagram; primitive definitions.

DEVELOPMENT DATA

```
                        ┌─────────────┐
                        │   STATE 0   │
                        └─────────────┘
                              │
                       ┌──────────────┐
                       │    POWER     │
                       └──────────────┘
                              │
                       ┌──────────────┐
                       │  LOAD  TE_NR │
                       └──────────────┘
                              │
                       ┌──────────────────┐
                       │ IF GATEWAY THEN  │
                       │   Vg : = TRUE    │
                       └──────────────────┘
                              │
                        ┌─────────────┐
                        │   STATE 1   │
                        └─────────────┘
                              │
                       ┌──────────────┐
                       │     RST      │
                       └──────────────┘
                              │
                       ┌──────────────────┐
                       │ ALLOWED : = TRUE │
                       └──────────────────┘
                              │
                         ┌───────────┐
                         │ FC : = INI │
                         └───────────┘
                              │
       yes            ◇─────────────◇
   ┌──────────────────│  Vg = TRUE  │
   │                  ◇─────────────◇
   │                              │ no
   │      yes     ◇──────────◇    │
   │  ┌───────────│   ANY    │    │
   │  │           │  SIGNAL  │    │
   │  │           ◇──────────◇    │
┌──────────┐          │ no        │
│   TOM    │          │           │
└──────────┘          │           │
   │                  │           │
   └──────────────┬───┴───────────┘
                  │
            ┌─────────────┐
            │   STATE 2   │
            └─────────────┘
                  │
```
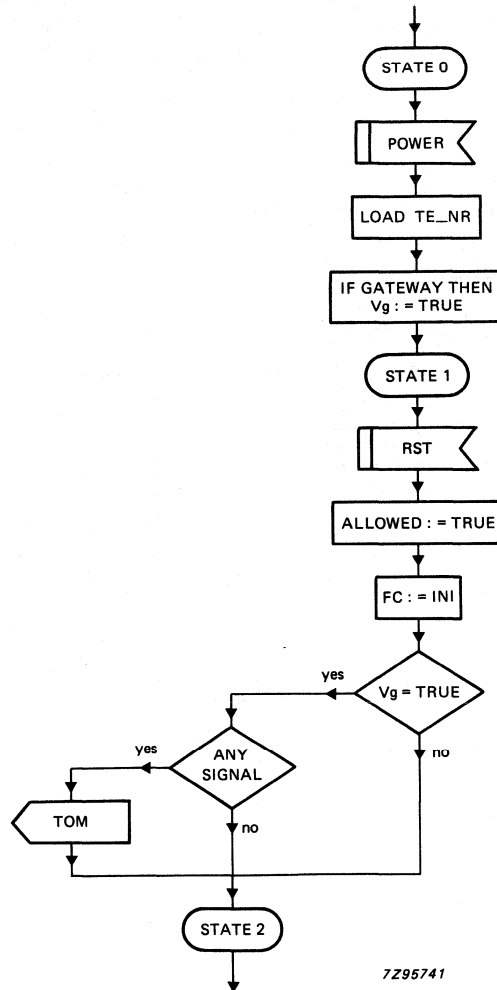
7Z95741

FC   = frame counter
INI   = initialization
RST   = reset
TE_NR   = terminal number

Where

At initialization the frame counter will be:

INI: $= (Vg \times 64 + TE\_NR) \times 256$

Fig. 7 Master/slave arbitration; part 1.

Fig. 8 Master/slave arbitration; part 2.

Where

SEND_FRAME: occupy frame channel and transmit "0011"
STOP_FRAME: release frame channel

FC = frame counter
INI = initialization
RST = reset

7Z95736

DEVELOPMENT DATA

STATE 0

POWER

SF : = 0

STATE 1

bd CHANNEL

OUT OF LOCK

FC : = 0

bd OCCUPIED — no

yes

FC = 1 — yes — no — FC = 16 AND SF = 1 — yes

FC : = 3 SF : = 0

no

FC = 3 — yes

SF : = 1

FC = 18 — no

yes

FC : = 17

FC : = FC + 1

FC : = 0

FC : = 0

7Z95740.1

Where

FC　= frame counter
SF　= "s" message flag

Fig. 9 bd channel access; frame counter.

START

STATE 0

s message

d message

see Fig. 12

RC : = 0

STATE 1

bd CHANNEL

RC = 0

yes / no

SF = 0

yes / no

RC = 1

no

RC = 2,3

no

FAILURE

v/FC = 3,16,18

no / yes

v/FC = 16,18

no / yes

FC = L − 1

no / yes

FC = H − 1

no / yes

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bd OCCUPIED

yes / no

STATE 2

Where

L   = 9 + decimal value of low order 3 bits of TE_NR
H   = 5 + decimal value of high order 2 bits of TE_NR
FC = frame counter
RC = retransmission counter
SF = "s" message flag

Fig. 10 bd channel access mechanism; part 1.

DEVELOPMENT DATA
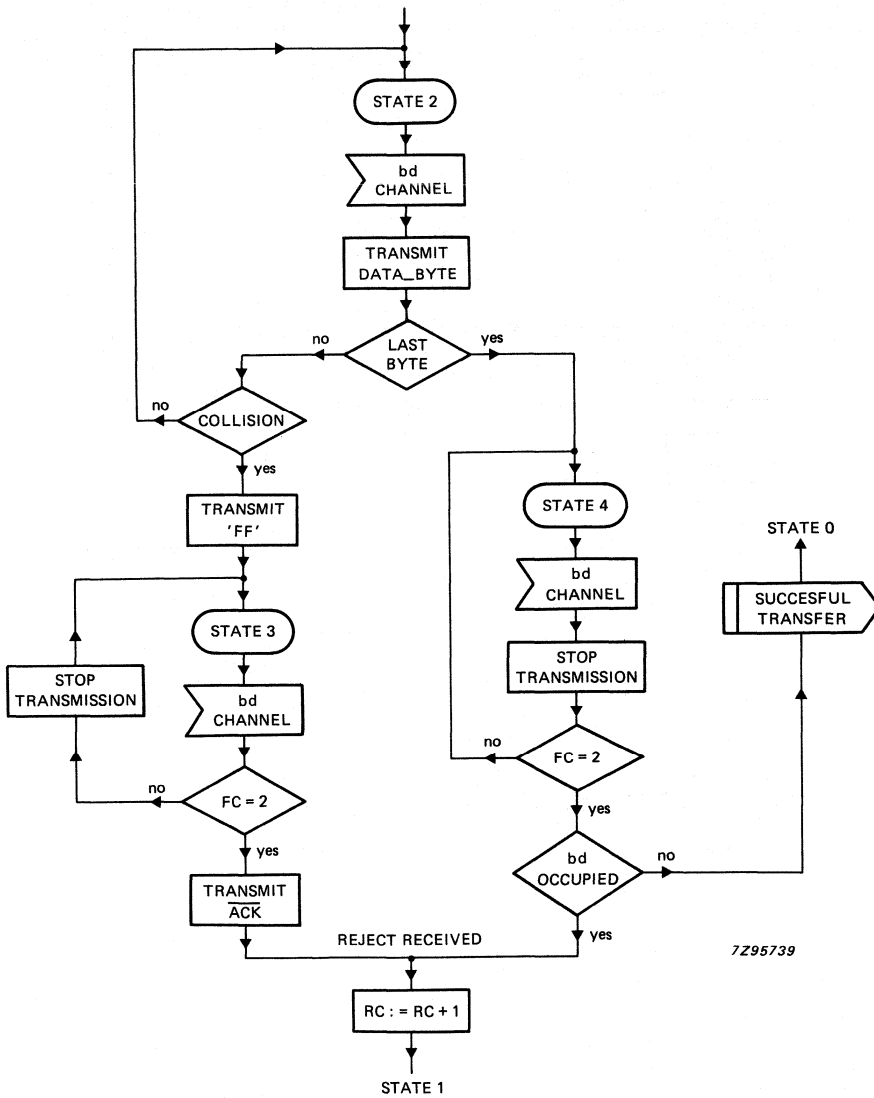
Where

FC = frame counter
RC = retransmission counter

Fig. 11 bd channel access mechanism; part 2.

START

STATE 0

d
message

s
message

RC : = 0

see Fig. 10

STATE 1

bd
CHANNEL

RC = 0 — no

yes

RC = 1 — no

yes

RC = 2 , 3 — no

yes

FAILURE

FC = 17 — no

yes

FC = L – 1
SF = 0 — no

yes

FC = H – 1
SF = 0 — no

yes

7Z95737

bd
OCCUPIED

yes

no

STATE 2

Where

L = 9 + decimal value of low order 3 bits of TE_NR
H = 5 + decimal value of high order 2 bits of TE_NR
FC = frame counter
RC = retransmission counter
SF = "s" message flag

Fig. 12 bd channel access mechanism; part 3.
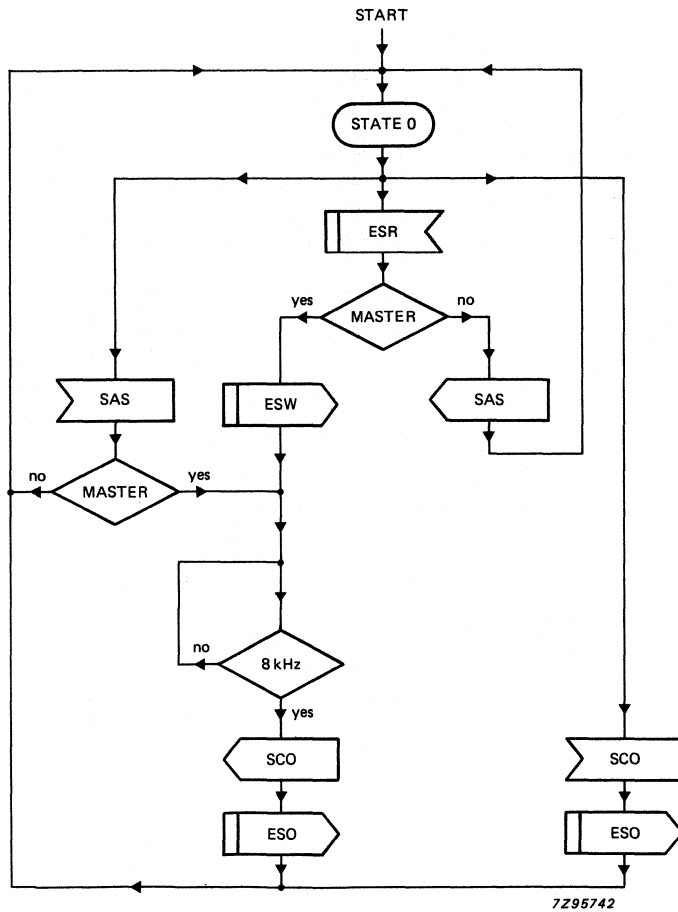
DEVELOPMENT DATA

Fig. 13 External synchronization; establishment procedure.

7Z95742
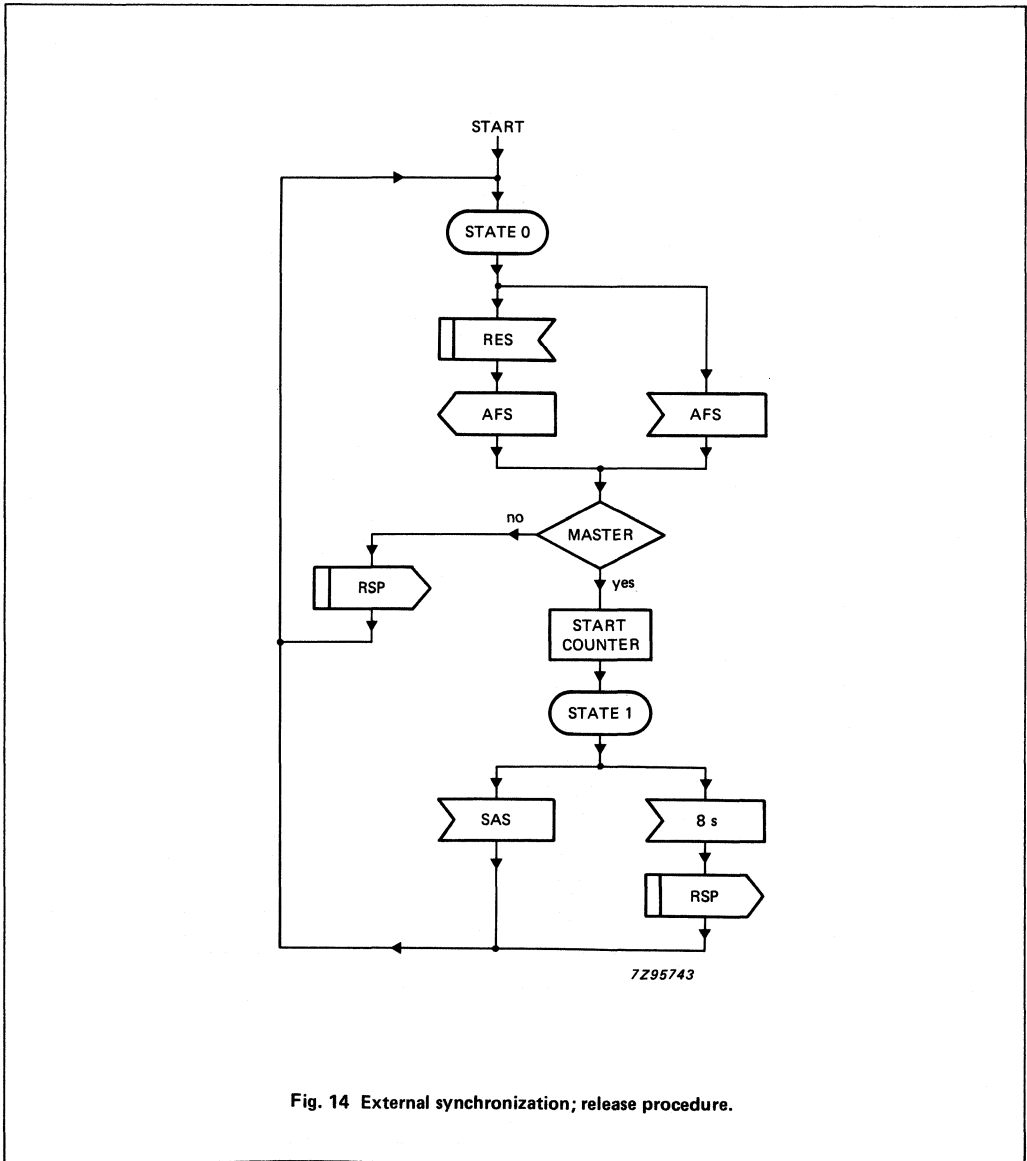
Fig. 14 External synchronization; release procedure.

7Z95743

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

PCB2310

IST BUS INTERFACE (IBI)

HOW TO USE THIS DATA SHEET

- **Section 1** introduces the IST bus interface. The
  functional areas of the circuit are shown with a block
  diagram and all input and output signals are described.
  The physical locations of the signals are indicated in
  a pinning diagram. Ordering information is found in
  this section.

- **Section 2** describes the functioning of the IST bus
  interface and follows the functional areas established by
  the block diagram in section 1. This section also describes
  how the functional areas are controlled by programmed
  instructions.

- **Section 3** provides the electrical characteristics. This
  section is used when designing system hardware.

- **Section 4** provides application information.

- **Section 5** gives details of the PCB2310 packaging.

CONTENTS

1.0 INTRODUCTION

The PCB2310 is a CMOS integrated VLSI circuit offering a full layer 1 and 2 interface for the IST bus. It operates as the interface between the IST bus at one side and at the other side it interfaces to intra terminal interfaces such as Terminal Highway (THW), Subscriber Line Data (SLD) bus and an 8-bit microcontroller with multiplexed address/data I/O lines.

The PCB2310 is one of a set of circuits required to complete the modular terminal architecture for Integrated Services Digital Network (ISDN) terminals. For contemporary analogue telephone functions the PCB2310 in conjunction with a signal processing codec filter requires only a microcontroller, a power supply, a transformer and some discrete components.

The IBI is an interface between different buses namely:

- The IST bus is a Local Area Network (LAN) with a maximum length of 300 metres (see IST bus specification). It offers a low-cost local communication medium for voice and data communications and is compatible with the ISDN according to CCITT-I series of recommendations. The IST bus can also be used with current analogue and digital networks.

- The SLD bus is a standardized 8 kHz synchronous communication bus for on-board routing of B, S and C channels. The C (control) and S (signalling) channels of the SLD bus are accessed via the microcontroller I/O port.

- The 8-bit microcontroller is a PCB80C51 compatible microcontroller bus. The data and address lines are multiplexed.

- The THW is a PCM highway with a transmission rate of 2.048 Mbit/s.

The eight 64 kbit/s circuit-switched IST bus channels are mapped on time slots on the THW which can be switched to the two B channels of the SLD bus. The 64 kbit/s packet-switched channel is routed to the 8-bit microcontroller parallel I/O port. The PCB2310 offers layer 1 and 2 services of the 7-layer hierarchy of the Open Systems Inter-connection (OSI) model developed by the International Standardization Organization (ISO) in this packet-switched channel of the IST bus.

Table 2.6-6 gives a quick reference to the PCB2310.

DEVELOPMENT DATA

1.1 Features

- Designed to interface with a twisted-pair cable via a coupling transformer for galvanic isolation and/or d.c. supply
- On-chip 8192 kHz clock generator
- 8 kHz synchronous frame
- External 8 kHz synchronization input for gateways
- Alternative Mark Inversion (AMI) line code
- Receiver input phase locked to the IST bus frame
- Automatic frame word transmitter allocation
- Eight 64 kbit/s half duplex circuit-switched channels which are fixed mapped on time slots of the Terminal Highway (THW)
- Three-wire 2 Mbit/s 32-channel Terminal Highway (THW):
  THDA: Terminal Highway data I/O 3-state pin
  THCL: Terminal Highway clock 2048 kHz clock input/output
  THSC: Terminal Highway synchronization 8 kHz input/output
- 4096 kHz and 8192 kHz clock output
- Three-wire 512 kbit/s 8-channel SLD bus:
  SIP   : SLD data I/O 3-state pin
  SCLK   : SLD clock input/output pin
  ESC/SDIR: 8 kHz synchronization input/output
- On-chip B channel switches and interface for SLD bus
- Time slot assignment control for the two B channels
- Distributed collision-free circuit-switched channel access mechanism, no central controller required
- Circuit-switched channel transfer facility for register recall services on duplex links
- One half duplex 64 kbit/s packet-switched common signalling and data channel (bd) with the following features:
  full layer 1 and 2 interface (OSI)
  single frame protocol
  immediate packet acknowledgement
  100% guaranteed channel access based on CSMA/CD (Carrier Sense Multiple Access/with Collision Detection)
  layer 2 service offers error-free packet transmission; transmission errors are recovered by re-transmissions
  error detection based on Frame Check Sequence (FCS) using Cyclic Redundancy Check (CRC) divider. The divider is:

$$X^{16} + X^{12} + X^5 + 1$$

  and the initial remainder is '00'
  separate program-sized transmit and receive buffers for signalling (s) packets and data (d) packets
  signalling packets have transmission priority over data packets
  flow control based on buffer availability

- 8-bit microcontroller I/O port including a 16-byte FIFO
- Access to S and C channels of SLD bus via 8-bit I/O port
- Maskable interrupt requests
- 21 control commands
- 13 control indications
- On-chip power-on reset circuit
- Monitor mode for bd channel
- Separate + 5 V supplies for analogue and digital parts

1.2 Ordering information

TYPE NUMBER	TEMPERATURE RANGE °C	PACKAGE
PCB2310WP	0 to +70	44-pin PLCC

DEVELOPMENT DATA
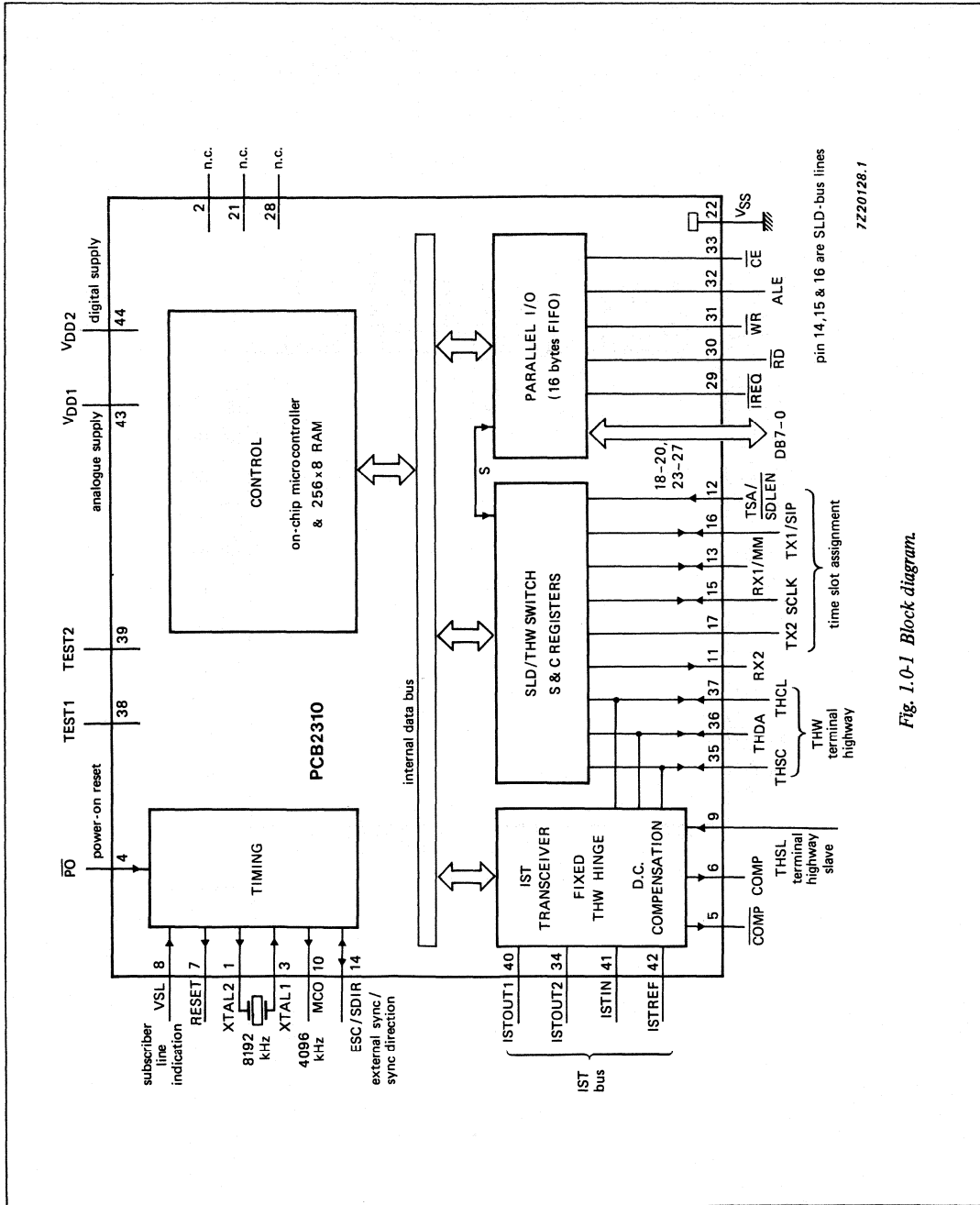
Fig. 1.0-1 Block diagram.

1.3 Signal description
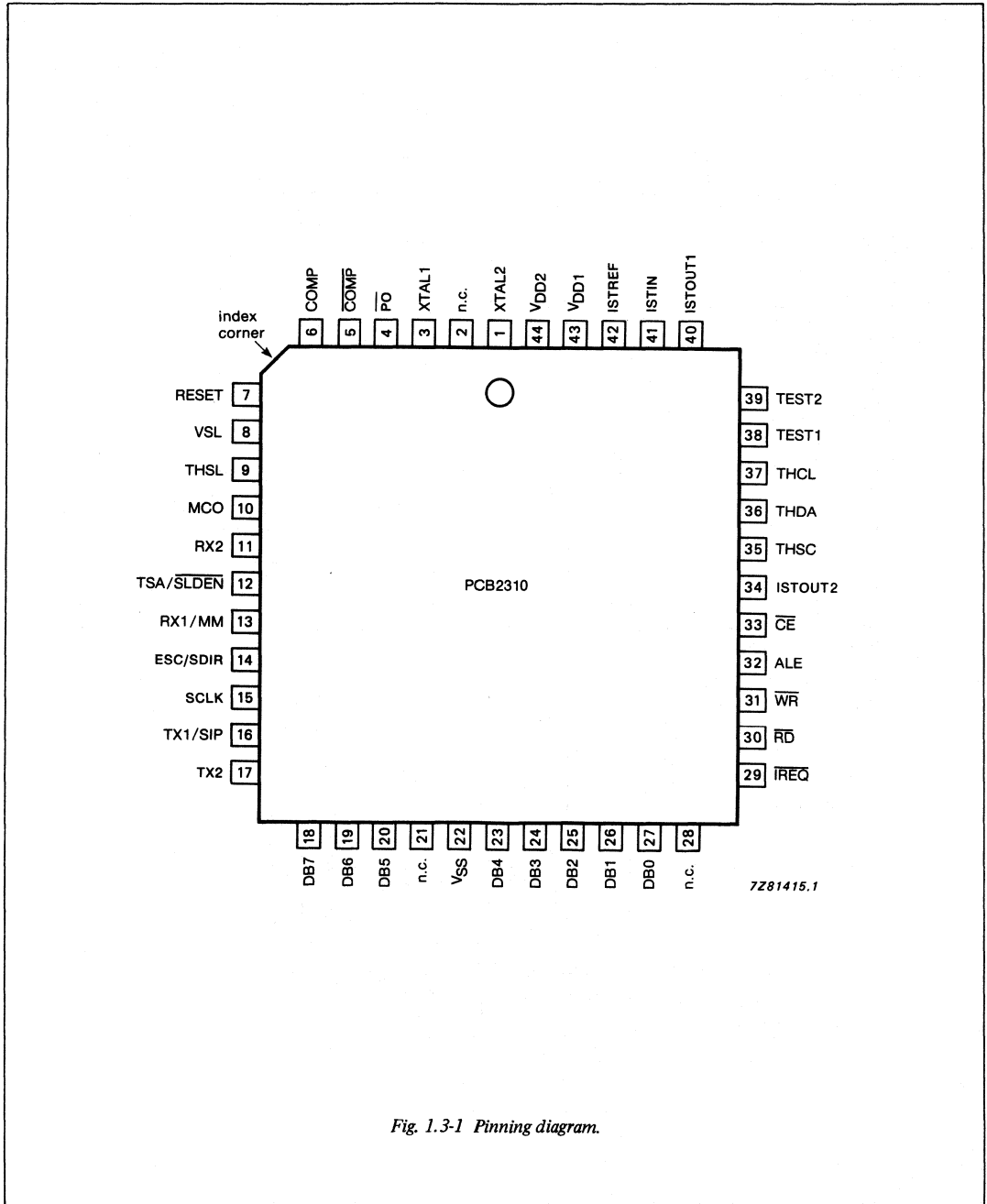
Fig. 1.3-1 Pinning diagram.

General

All inputs except $\overline{PO}$ are TTL compatible.
Unless otherwise specified all outputs can drive 2 TTL
(= 8 LSTTL) inputs and equivalent CMOS inputs.

1 XTAL2   Inverting buffer output; part of clock
generator circuit. One side of the crystal is
connected to pin 1 via a resistor of 1 kΩ.
This pin could drive other circuits provided
the capacitive load is less than 15 pF (see
section 2.11). When using an external
clock generator pin 1 is not connected.

2 n.c.   not connected.

3 XTAL1   Inverting buffer input. The other side of the
crystal is connected to pin 3. An 8192 kHz
± 100 ppm crystal must be used. An external
clock generator can also be connected to
this pin.

4 $\overline{PO}$ Power On/reset active LOW* input. If there
is a LOW pulse of > 1 μs, while the clock is
running, the PCB2310 will be reset. If pin 4
is HIGH it will be automatically reset by an
internal circuit provided the voltage on
V_{DD1} (pin 43) is < 1,2 V and rising to 5 V
with a slope > 5 V/ms.

5 $\overline{COMP}$ Compensation active LOW output.

6 COMP   Compensation active HIGH output.
These two outputs are used to compensate
the change in inductive current in the
transformer (Fig. 4.0-3).

7 RESET   Active HIGH output. If RESET = HIGH
the PCB2310 is performing an internal reset.
Pin 7 could also be used to reset the
microcontroller. After power up this pin
will be HIGH for 1 ms.

8 VSL   Subscriber line connection input.
VSL = HIGH indicates that the PCB2310 is
part of a gateway to other network(s) such
as ISDN 'S reference point'.

9 THSL   Terminal highway slave mode selection input.
THSL = LOW puts the Terminal Highway
(THW) interface to the normal master mode.
THSL = HIGH switches the PCB2310 to the
slave mode on the Terminal Highway. In this
mode THCL (pin 37) and THSC (pin 35) are
external inputs.

10 MCO   Master clock output (4096 kHz). This
output can be used as a clock output to drive
peripheral circuits. The output is the crystal
frequency divided by 2 with a duty cycle of
50%.

11 RX2   THW time slot assignment output.
RX2 = HIGH during time slot on the THW
that is set by the command <SBS> (see
section 2.7.5).

12 TSA/   Input signal to select between time slot
$\overline{SLDEN}$ assignment and SLD bus signals. If
TSA = LOW pins SIP (pin 16)
and MM (pin 13) are in the SLD mode. If
TSA = HIGH these pins are switched to Time
Slot Assignment mode.

13 RX1/MM   THW time slot assignment output/Master
Mode selection input. If TSA = HIGH, this
pin is an output, and the signal is HIGH
during the time slot on the THW that is set
by the command <SBS>.

If in the SLD mode (TSA = LOW) this is an
input pin and selects between the master
mode or the slave mode on the SLD bus:
MM = HIGH = Master mode;
MM = LOW = Slave mode.

14 ESC/   External synchronization/Frame
SDIR   synchronization input/output. If in the
master mode on the SLD bus (MM = HIGH
and TSA = LOW) this pin is an output for
the 8 kHz synchronization signal of the SLD
bus. If in the slave mode or in the TSA mode
(MM = LOW or TSA = HIGH) this pin is an
input and the PCB2310 synchronizes on to
the 8 kHz ESC signal if VSL = HIGH and the
PCB2310 is master on the IST bus.

15 SCLK   SLD clock input/output.
If master on the SLD bus (TSA = LOW;
MM = HIGH) SLCK provides the 512 kHz
clock signal, if slave (TSA = LOW;
MM = LOW) the 512 kHz clock is input
to this pin.

* LOW means voltage on pin 4 is equal to V_{SS} (pin 22).
  HIGH means voltage on pin 4 is equal to V_{DD2} (pin 44).

DEVELOPMENT DATA

1.3 Signal description (continued)

16 TX1/ SIP THW time slot assignment output/SLD data I/O** pin. If TSA = HIGH this pin is an output, and the signal is HIGH during the time slot on the THW that is set by the command <SBS>.

If slave on the SLD bus (TSA = LOW; MM = LOW) data can be transmitted in the B_1 and B_2 channels when SDIR (pin 14) is LOW and in the other channels when the output is 3-state.
Both B_1 and/or B_2 channels can be programmed to output a high impedance.

If master on the SLD bus (TSA = LOW; MM = HIGH) the B_1, B_2, S and C channels are transmitted when ESC is HIGH. Data is put on the SIP output at a positive transition of SCLK. The idle code in the B_1, B_2 and C channels is all logic 1's and in the S channel the initial code is all logic 0's.

17 TX2 THW time slot assignment output. TX2 is HIGH during the time slot on the THW that is set by the command <SBS>.

18-20 23-27 DB7-0 Combined address input and data I/O port. These pins are used to access internal registers P80 to P83. The selection between address and data is made by ALE (pin 32). $\overline{WR}$ (pin 31) and $\overline{RD}$ (pin 30) will select input or output respectively.

21 n.c. not connected.

22 V_{SS} Ground.

28 n.c. not connected.

29 $\overline{IREQ}$ Interrupt request is an open drain output. This signal is active LOW. If a bit is set in the interrupt register P80, pin 29 is made LOW. If the interrupt is serviced by reading register P80 the interrupt will be reset.

30 $\overline{RD}$ Read active LOW input. If this input is LOW data from the addressed register will be put on the DB7-0 I/O port.

31 $\overline{WR}$ Write active LOW input. If this input is LOW data on the DB7-0 I/O port will be written into the addressed register.

32 ALE Address latch enable input. A HIGH on this pin latches the data on the DB7-0 I/O port into the address latch provided $\overline{CE}$ (pin 33) is LOW.

33 $\overline{CE}$ Chip enable active LOW input.

34 ISTOUT2 IST bus output pin. 3-state output, capable of directly driving the IST bus. Complementary to ISTOUT1 (pin 40).

35 THSC Terminal highway synchronization input/output. When THW interface is in master mode (THSL = LOW) pin 35 outputs a pulse with a duration of one 2048 kHz cycle and a repetition frequency of 8 kHz. When THW interface is in slave mode (THSL = HIGH) pin 35 becomes an input. If monitor mode is selected (see section 2.10), pin 35 outputs a strobe to monitor the bd receive channel.

36 THDA Terminal highway data I/O** pin. Data is put on this line on a positive transition of THCL (pin 37).

37 THCL Terminal highway clock input/output pin. This output can drive 4 TTL (= 16 LSTTL) inputs. When THW interface is in master mode this pin provides a 2048 kHz clock. When THW interface is in slave mode this pin is the input for a 2048 kHz clock.

38 TEST1
39 TEST2 These pins are for production test and both must be LOW for normal operation.

40 ISTOUT1 IST bus output pin. 3-state output, capable of directly driving the IST bus. Complementary to ISTOUT2 (pin 34).

41 ISTIN IST bus input pin (input of the IST bus receiver, see section 2.3 and IST bus specification).

42 ISTREF IST bus reference pin. This pin outputs a voltage of $V_{DD2}/2 \pm 60$ mV.

43 V_{DD1} Supply voltage for the analogue parts of the PCB2310. $V_{DD1} - V_{SS} = 5$ V $\pm 5\%$.

44 V_{DD2} Supply voltage for the digital parts of the PCB2310. $V_{DD2} - V_{SS} = 5$ V $\pm 5\%$.

** I/O indicates a 3-state pin; HIGH, LOW or high impedance.

2.0 FUNCTIONAL DESCRIPTION

2.1 General description

The PCB2310 performs the electrical interface and the protocols on the IST bus as described in the IST bus specification. A brief description of the IST bus is given in section 2.2.

The circuit-switched channels on the IST bus (b1 to b8) are mapped on specific Terminal Highway (THW) time slots and can be routed to SLD B_1 and B_2 channels and vice versa.

$$\text{IST b1 to b8} \xleftrightarrow{\frac{\text{FIXED}}{\text{MAPPING}}} \text{THW} \xleftrightarrow{\frac{\text{CONTROLLABLE}}{\text{ALLOCATION}}} \text{SLD} (B_1, B_2)$$
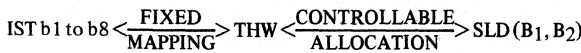
The packet-switched bd channel on the IST bus is routed through layer 1 and layer 2 entity. The service access point on the layer 2 service is performed by the microcontroller I/O port.

The microcontroller I/O port performs the interface for the control stages of the PCB2310 and is also the access point for the C and S channels on the SLD bus.

An on-chip reset circuit and clock generator minimizes the number of external components.

2.2 IST bus description

The PCB2310 is fully developed to operate according to the IST bus specification. The PCB2310 can be connected direct to the IST bus via a transformer.

The 8 kHz (125 μs) synchronous IST bus frame contains ten time division multiplexed channels as shown in Fig. 2.2-1:

- 1 x 5-bit synchronization channel; Frame (F)
- 1 x 64 kbit/s packet-switched channel; Data (bd)
- 8 x 64 kbit/s circuit-switched channels; Data/voice (b1 to b8)

Each channel is preceded with an 'occupied' bit which is logic 1 if the channel is occupied.

2.2.1 bd channel

The PCB2310 interfaces the bd channel with the 8-bit microcontroller I/O port, for which it performs a full layer 1 and 2 service as defined in the IST bus specification. It performs all the requirements for error detection and correction by re-transmissions and flow control on the packets transmitted in the bd channel. Layer 2 packets for re-transmission can be stored in the 256 x 8 internal RAM.
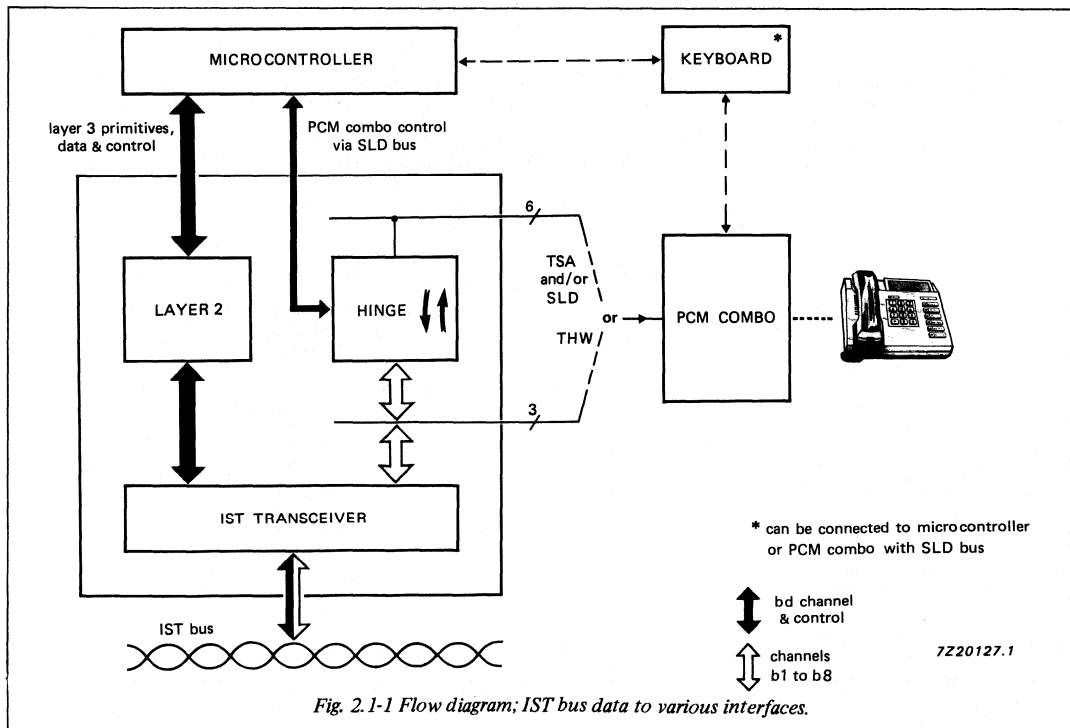
Fig. 2.1-1 Flow diagram; IST bus data to various interfaces.

2.2.2 b channels

The PCB2310 also handles the circuit-switched channel connections; the access mechanism being completely distributed. There is no network manager. Command <FFC> (see Table 2.6-6) orders the PCB2310 to access a free b1 to b8 circuit-switched channel. A b1 to b8 channel is fetched by transmitting an 'occupied' bit (see Fig. 2.2-1) and the data on the corresponding THW time slot will be mapped upon this IST bus b1 to b8 channel. With command <OAR> the ordered channel will be occupied as soon as it is released.

A channel is seen **free** if the 'occupied' bit of that channel is logic 0 for at least **two consecutive frames.**
A channel is seen **released** if the 'occupied' bit is logic 0 for at least **one frame.**

2.2.3 Frame channel

The PCB2310 can operate on the IST bus in two modes; master or slave. In the PCB2310 the complete distributed master/slave arbitration protocol is implemented (see IST bus specification). All IST slaves will synchronize on the frame channel as transmitted by the IST master. If VSL (pin 8) is HIGH and the PCB2310 is master on the IST bus,

the PCB2310 will synchronize on the 8 kHz external input signal at ESC/SDIR (pin 14).

The PCB2310 also performs some maintenance functions such as IST BUS_DOWN and IST BUS_UP.

2.3 IST bus I/O stage

The IST bus I/O stage consists of a receiver and a transmitter. The line code is Alternative Mark Inversion (AMI).
The bit rate is 1024 kbit/s based on an 8192 kHz crystal. ISTOUT1 (pin 40) and ISTOUT2 (pin 34) drive the IST bus while ISTREF (pin 42) is held at $V_{DD}/2 \pm 60$ mV.
To buffer ISTREF an external 100 nF capacitor should be connected between pin 42 and V_{SS}. To handle the IST bus specification a transformer with a ratio —
IST bus: PCB2310 = 1 : 2 is required.

ISTIN (pin 41) is the input for the receiver comparator. The comparator reference voltage is derived from the voltage on pin 42. There is hysteresis built in to the comparator.
The comparator can handle input pulse limits as defined in Fig. 2.3-1.
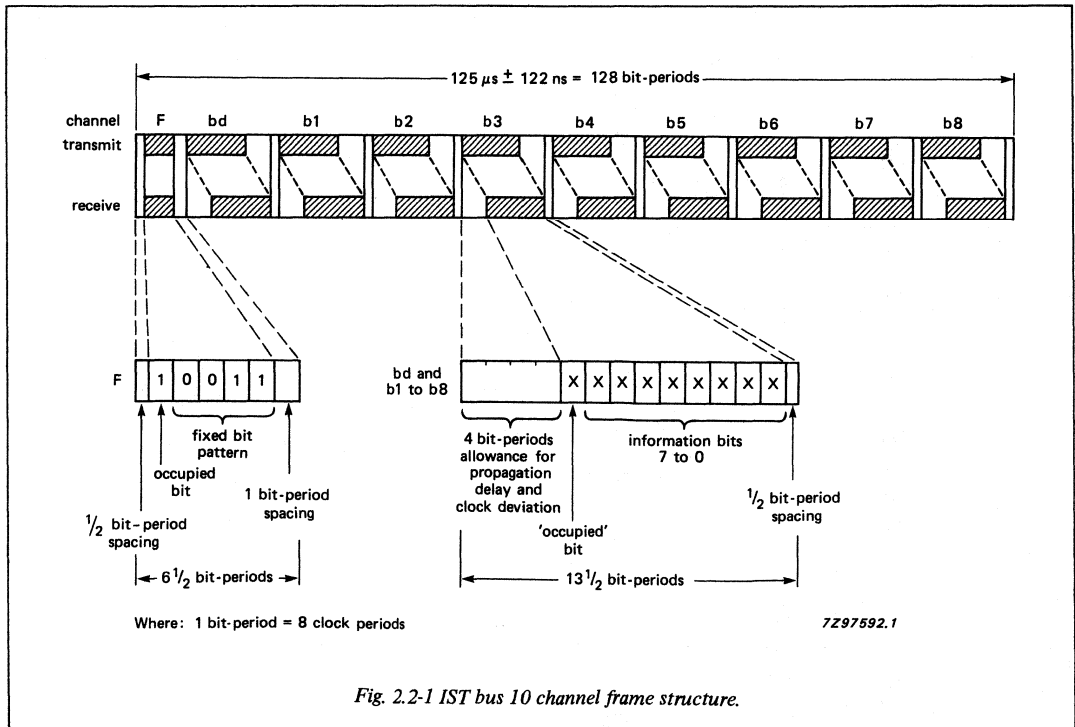
Fig. 2.2-1 IST bus 10 channel frame structure.

DEVELOPMENT DATA
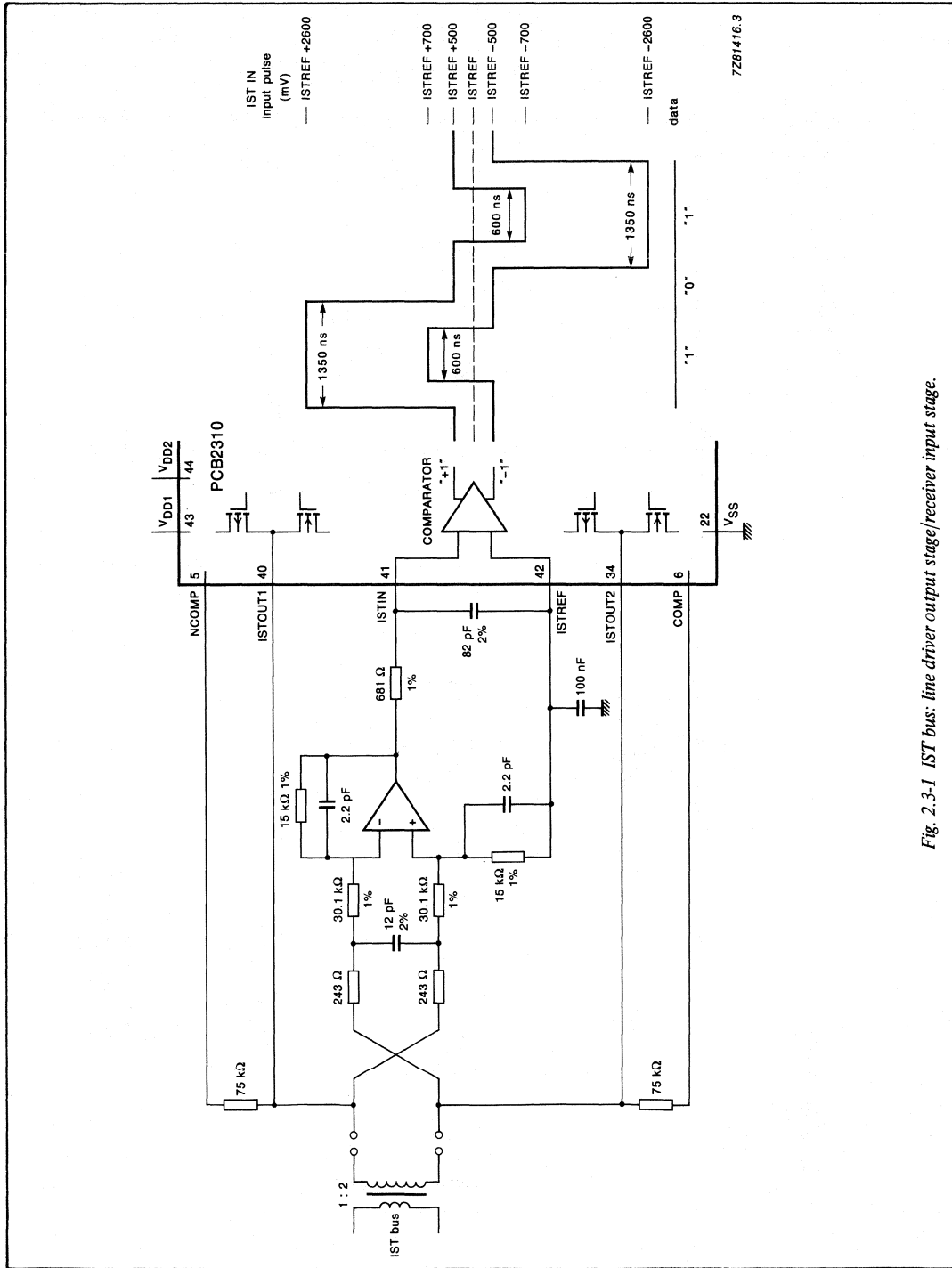
Fig. 2.3-1 IST bus: line driver output stage/receiver input stage.

Fig. 2.4-1 IST <----> THW mapping.
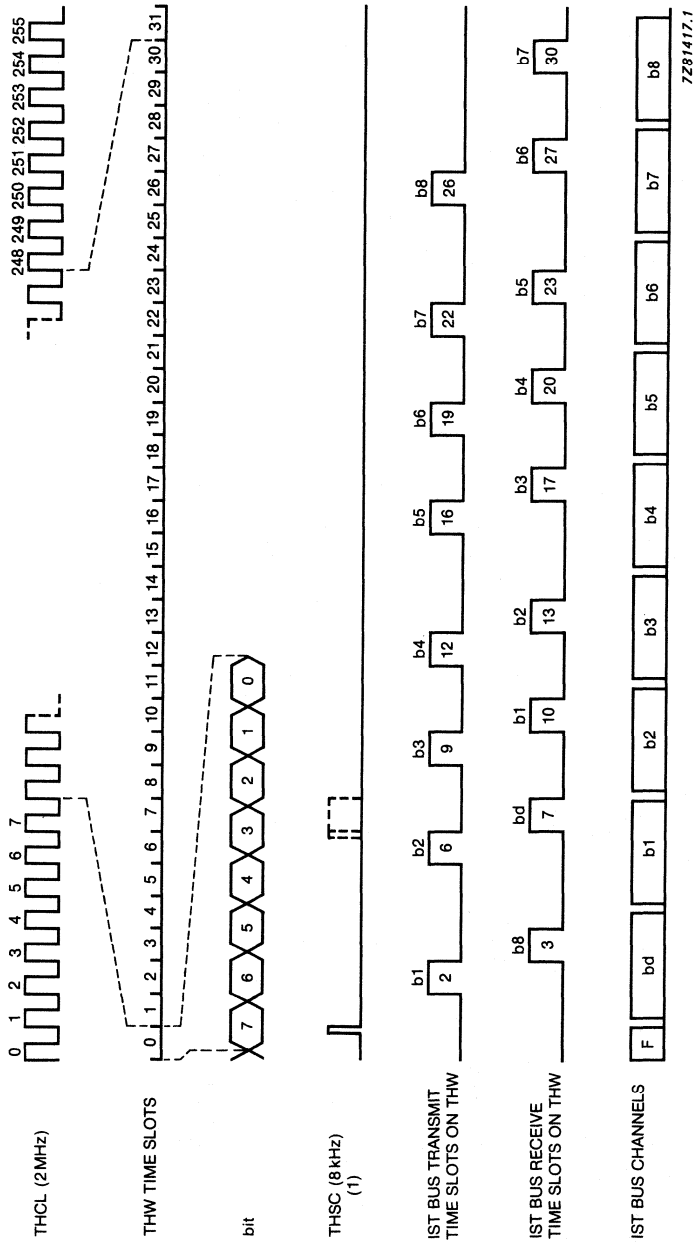
(1)

THW normal mode — THSC falls over bit 1 of THW time slot 0.
THW monitor mode (IST bd not occupied) — THSC falls over bit 0 of THW time slot 6.
THW monitor mode (IST bd occupied) — THSC falls over bit 0 of THW time slot 6 and bit 7 to 0 of time slot 7.

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DEVELOPMENT DATA

2.4 Terminal highway interface

The Terminal Highway (THW) is a 2 Mbit/s three-wire full duplex PCM highway for 64 kbit/s circuit-switched channels. The THW will normally be used to interconnect a PCM codec filter or a data terminal that transmits in one of the IST b1 to b8 channels.

The THW offers 32 time slots, 17 of which are used to transmit and receive the IST bus channels. Channels b1 to b8 and bd are mapped upon fixed time slots on the THW (see Fig. 2.4-1). The remaining 14 time slots are 'free'. The THDA data is clocked with the 2048 kHz clock. However, time slots 0 and 31 may be temporarily clocked with a clock period that varies by 25% for synchronization.

The THW interface can operate in 3 separate modes:

- Master
- Slave
- Monitor

When THSL (pin 9) is LOW either the THW master mode or the THW monitor mode is selected. When THSL is HIGH the THW slave mode is selected. The distinction between THW master mode and THW monitor mode is made by setting bit 2 of internal register RR06. If this bit is HIGH the monitor mode is selected. This register can be accessed using the <LOR> command (see Table 2.7-2 Register allocation).

In the master mode the PCB2310 provides the THW bus with a 2048 kHz clock output (THCL; pin 37) and an 8 kHz synchronization output (THSC; pin 35). See Fig. 3.3-1 THW timing.

The THW monitor mode can be used to monitor the bd channel on the IST bus. In this mode the PCB2310 provides a time slot assignment signal on the 8 kHz synchronization output (THSC; pin 35). If the bd channel on the IST bus is occupied the THSC sync pulse is extended with a strobe. This strobe-signal falls over time slot THW 7.

When several PCB2310s are connected together (e.g. by a PCM 30 switch) the THW slave mode is used. In this mode the terminal highway synchronization input (THSC; pin 35) and the clock input (THCL; pin 37) are provided by peripheral circuits. In this application the PCB2310 is frequency and phase locked to the external inputs, and will be master on the IST bus. The consequence of this application is that only one terminal connected to the same IST bus can have a slave connection on the THW (see Fig. 4.0-2d). The master and slave must operate with the same 8192 kHz crystal clock.

2.5 SLD bus interface/time slot assignment outputs

Pins 14, 15 and 16 perform either the SLD interface or the time slot assignment on the THW. Mode selection is defined by TSA/$\overline{\text{SLDEN}}$ (pin 12); TSA/$\overline{\text{SLDEN}}$ = HIGH selects time slot assignment mode (TSA).

2.5.1 TSA mode

In the TSA mode pins 11, 13, 16 and 17 output strobe pulses that fall over specific time slots on the THW. These strobe pulses can be used to clock data to and from the THW. The time slots will be set by command <SBS> (see section 2.7.5).

2.5.2 SLD mode

When TSA/$\overline{\text{SLDEN}}$ is LOW the SLD feature switch is selected. The SLD bus is used to connect B channel devices, such as interfaces to other networks or codecs. The B$_1$ and B$_2$ channels of the SLD bus can be switched to any of the THW time slots by the SLD switch. In this way it is possible to map IST b1 to b8 channels via the THW onto the SLD B$_1$, B$_2$ channels, and vice versa.

$$\text{IST b1 to b8} \xleftarrow{\frac{\text{FIXED}}{\text{MAPPING}}} \text{THW} \xleftarrow{\frac{\text{CONTROLLABLE}}{\text{ALLOCATION}}} \text{SLD} (B_1, B_2)$$

The selection of channels is programmable via the microcontroller I/O port with command <SBS> (see section 2.7.5).

In the SLD mode the PCB2310 can be master or slave on the SLD bus. If TSA = LOW and MM = HIGH the SLD master mode is selected. If TSA = LOW and MM = LOW the SLD slave mode is chosen.

2.5.3 Combined TSA and SLD mode

If the output from the SLD B2 channel is not used this output can be disabled by the 'd' bit (see Table 2.6-6 Register P82; I/O control commands), the RX2 output (pin 11) can be programmed over any THW time slot. In the same way the output from the SLD B2 channel to the programmed THW time slot can be disabled, then the TX2 output (pin 17) can be programmed over any THW time slot.

2.5.4 Master mode

In the master mode the SLD bus is provided with the 512 kHz clock signal (SCLK; pin 15) and the 8 kHz synchronization signal (ESC/SDIR; pin 14). In the master mode the PCB2310 controls the SLD bus and thus the PCM codec filter connected to it. In the slave mode the PCB2310 expects an externally provided clock and synchronization signal.
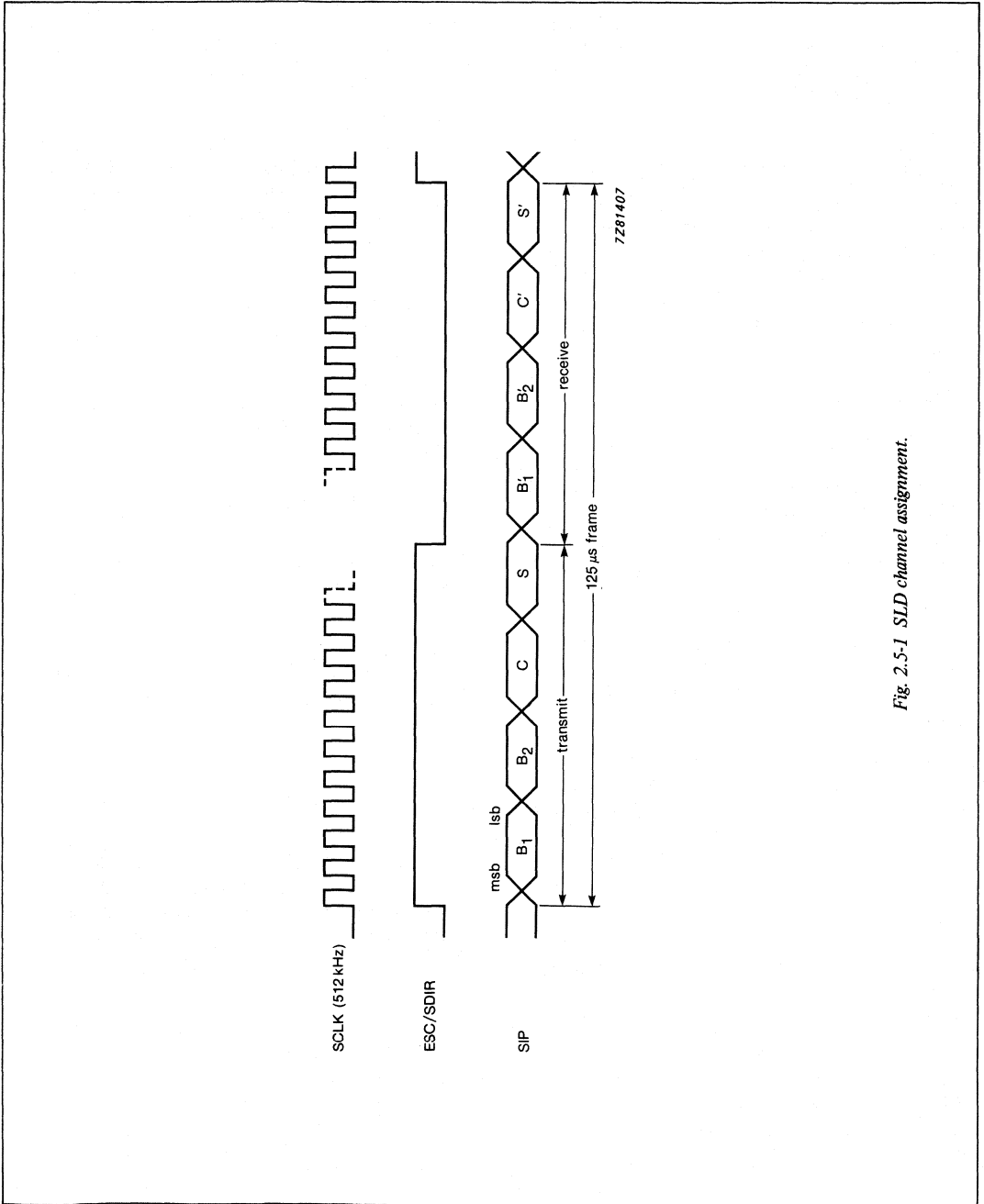
Fig. 2.5-1 SLD channel assignment.

In the master mode the B_1, B_2, C and S channels are transmitted by the PCB2310 when ESC/SDIR is HIGH. The idle code for B_1, B_2 and C channels is all logic 1's and for the S channel all logic 0's. When ESC/SDIR is LOW the SIP output pin is high impedance and data can be received on the SIP pin (see Fig. 2.5-1).

A microcontroller can control the duplex C channel via the control path of the PCB2310. The consecutive control bytes can be loaded into the PCB2310 by command <SCT>. The PCB2310 inserts an NOP code (= hex FF) when no information is offered by the microcontroller for transmission in this channel.

The PCB2310 provides a transparent transmit and receive path for the microcontroller onto the duplex S channel via the I/O register P83. The receive path is equipped with a last-look detector.
A maskable interrupt request ($\overline{\text{IREQ}}$) is generated by:

- Any data contents change
- Any byte being transmitted in the S transmit channel

2.5.5 Slave mode

In the slave mode the PCB2310 acts similar to an SLD codec. Another device must be master on the SLD bus. In the slave mode the PCB2310 can be programmed to transmit on either one or both the B_1 and B_2 channels when ESC/SDIR is LOW. The S and C channel outputs are high impedance.

The PCB2310 synchronizes on to the 8 kHz ESC/SDIR signal if it is IST master, SLD slave and VSL = HIGH.

2.6 8-bit microcontroller bus

The PCB2310 is completely controllable by the 8-bit microcontroller bus which is compatible with the MAB80C51 8-bit microcontroller bus.

The bus consists of:

- 8 data/address multiplexed I/O lines (DB7 to DB0; pins 18 to 20 and 23 to 27)
- An interrupt request output ($\overline{\text{IREQ}}$; pin 29)
- A read input ($\overline{\text{RD}}$; pin 30)
- A write input ($\overline{\text{WR}}$; pin 31)
- An address latch enable input (ALE; pin 32)
- A chip enable input ($\overline{\text{CE}}$; pin 33)

When ALE is HIGH and $\overline{\text{CE}}$ is LOW, data on the DB7-0 I/O port is latched into the address latch. One from four internal registers (P80 to P83; see Fig. 2.6-1) is selected. The PCB2310 stores, then writes the data-byte from the data-bus I/O port into the addressed register (see Table 2.6-1).
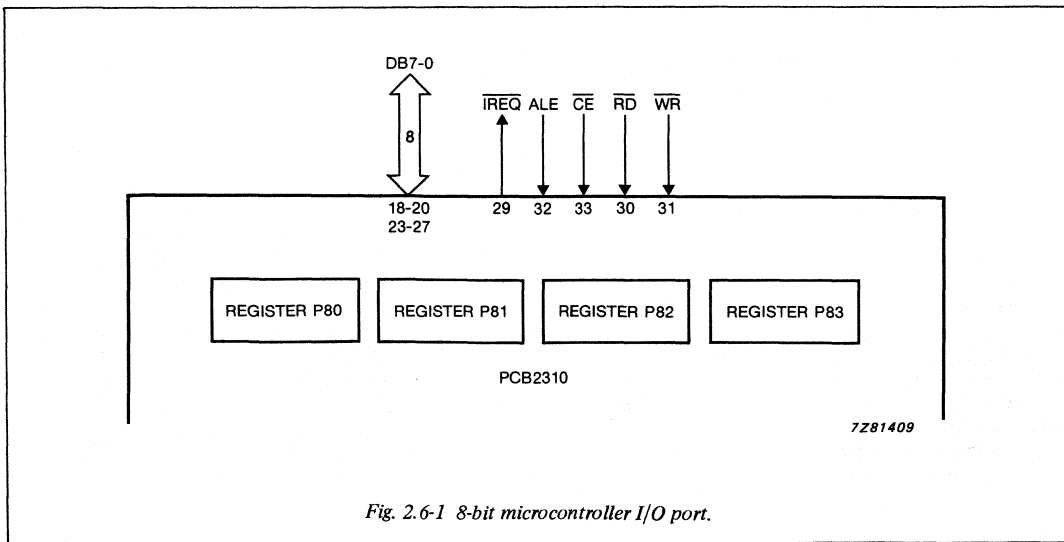
Fig. 2.6-1 8-bit microcontroller I/O port.

Table 2.6-1 Register addresses

REGISTER	ADDRESS							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P80	1	0	0	0	0	0	0	0
P81	1	0	0	0	0	0	0	1
P82	1	0	0	0	0	0	1	0
P83	1	0	0	0	0	0	1	1

The P80 to 83 registers have the following functions:

- P80; PCB2310 interrupt vector/mask register
- P81; parallel I/O status/control register
- P82; main IST bus control, bd channel and SLD (C) channel I/O port (including a 16-byte FIFO)
- P83; S channel I/O of SLD bus

2.6.1 Registers P80, P81 (see Table 2.6-2)

The PCB2310 generates maskable interrupt requests ($\overline{\text{IREQ}}$) if:

- A different information byte has been received on the S'channel of the SLD bus

and

- The last byte loaded in register P83 has been transmitted in the S channel on the SLD bus for the first time
- The FIFO is loaded with data waiting for transfer to the microcontroller
- The FIFO is waiting for more information during input mode

The microcontroller interface can be used in two modes or a mixture of both:

- Polling mode
- Interrupt mode

2.6.1.1 Polling mode

When using the polling mode all masked bits of register P80 (bits D7 to D3) must be set to logic 0. When using the mixed mode some bits could be set to logic 1.

In the polling mode the microcontroller polls each peripheral device that is connected to it. When polling the PCB2310 it reads register P81 (no status bits are reset when polling register P81).

Table 2.6-2 Bit assignment; register P80, P81

COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
read P80	IDIR	IDOR	IRDR	ISSR	ISST	NB2	NB1	NB0
write P80	MDIR	MDOR	MRDR	MSSR	MSST			
read P81	DIR	DOR	BCE	SSR	SST	NB2	NB1	NB0
write P81	ETR	DRQ						

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Table 2.6-3 Register P81; polling bits

BIT	ACTION
read	
DIR*	Data Input Request indicates FIFO is free for next part of the message ($\leqslant$ 16 bytes). This bit will be reset if the microcontroller writes to register P82 FIFO or whenever an ETR or DRQ instruction is given. A write request to P82 FIFO should always end with a ETR or DRQ bit being written to P81.
DOR*	Data Output Request indicates that there is data waiting for output to the microcontroller. If BCE is logic 0 then the PCB2310 initiated the data transfer. If DOR is set, the BCE bit is set as well if it is a response to a mode b I/O command terminated with a DRQ. DOR bit will be reset by reading the P82 FIFO or by writing ETR or DRQ bit to P81. Writing to P82 FIFO will overrule the data output request. Reading the P82 FIFO should always end by writing ETR bit to P81 except when the PCB2310 initiated the data transfer and all bytes (NB2 to NB0) have been read.
SSR*	SLD Signalling byte Received indicates that a change has been detected in the bytes coming from the SLD S' channel. The last byte will be held until read by the microcontroller. The data in the SLD S' register is valid if SSR is asserted. This bit will be reset by reading the P83 register.
SST*	SLD Signalling byte Transmitted. The byte, last loaded by the microcontroller, has been transmitted to the SLD S channel. This bit is set to logic 0 if a new byte is loaded in the P83 register.
BCE	Busy on Command Execution indicates that a mode a or b I/O command is in progress. No new command may be entered until BCE is negated. This bit is set when a command is entered and reset when the command has been interpretted and handled. If the microcontroller is fetching data from the PCB2310, BCE remains logic 1 until the read cycle is ended with ETR being written to P81.

Table 2.6-3 (continued)

BIT	ACTION
NB2 to NB0	This indicates the number of bytes in the FIFO in the event of a Data Output Request being initiated by the PCB2310 (BCE = logic 0). A data output request initiated by the microcontroller will always result in 16 bytes being loaded in the FIFO by the PCB2310; thus NB2 to NB0 will have no meaning.
write	
ETR	End of transmission. The microcontroller must set this bit to indicate the end of transmission. This applies to the PCB2310 writing or reading data to the P82 FIFO. If ETR is issued during a PCB2310 data output phase that was initiated by the PCB2310 and bytes NB2 to NB0 have not all been read, the P82 FIFO will be cleared and then a new trial will attempt to output the interrupted data.
DRQ	Data request. With this signal the microcontroller indicates to the PCB2310 that it will switch the transmission direction from WRITE to READ. It will force the PCB2310 to fill the FIFO with appropriate data and the DOR bit to be set while BCE is at logic 1.

2.6.1.2 Interrupt mode

In Table 2.6-3 all bits marked with an asterisk will generate an interrupt if asserted. If more interrupts are asserted at the same time only one is marked in register P80; the others are pending. However, in register P81 all valid bits are written.

Table 2.6-4 Register P80; interrupt bits

BIT	ACTION
write	
MDOR	Mask interrupt IDOR if asserted
MRDR	Mask interrupt IRDR if asserted
MDIR	Mask interrupt IDIR if asserted
MSSR	Mask interrupt ISSR if asserted
MSST	Mask interrupt ISST if asserted
	condition: power on; all masks set to logic 0; all interrupts disabled.
read	
ISSR	set if SSR x MSSR x priority is true
ISST	set if SST x MSST x priority is true
IDIR	set if DIR x MDIR x priority is true
IDOR	set if DOR x MDOR x $\overline{BCE}$ x priority is true
IRDR	set if DOR x MRDR x BCE x priority is true (RDR means Requested Data Ready)
	priority: ISSR has priority over ISST. ISST has priority over IDIR, IDOR and IRDR. IDIR and IDOR and IRDR are mutually exclusive and will not occur at the same time. $\overline{IREQ} = (IDIR + IDOR + IRDR + ISSR + ISST)$

Interrupt bits will be reset by reading P80.

2.6.2 Register P82; FIFO data path

Register P82 is the main IST bus control, bd channel and SLD (C) channel I/O port. It includes a 16-byte FIFO for adaptation to the 8 kbyte/s processing capability of the PCB2310. The PCB2310 is a multi-function device which requires a CONTROL byte <CTRL> after P82 has been addressed, to select between the various chip functions. <CTRL> can be followed by a PARAMETER byte(s) <PAR> for extension of the data destination address (pointers, channel numbers etc.). The PCB2310 can transfer data to the microcontroller by its own initiation, or when initiated by the microcontroller.

Table 2.6-5 displays the protocol that is implemented on register P82 FIFO address. There are 3 modes: a, b and c.

- a: PCB2310 input
- b: PCB2310 input/output
- c: PCB2310 output

Before entering new commands to PCB2310 register P82 (MODE A or B), register P81 bits BCE, NB2, NB1 and NB0 must be at logic 0. If NB2, NB1 or NB0 are at logic 1 MODE C will be indicated in progress. In this event wait until the DOR bit is set to execute the MODE C indicate (via an interrupt or on polling base).

Table 2.6-5 Register P82; I/O commands

MODE	PROTOCOL
PCB2310 input initiated by microcontroller (< 16 bytes)	
a	P82 write <CTRL>[<PAR>] [<DATA>] ; P81 write ETR.
b	P82 write <CTRL>[<PAR>] [<DATA>] ; P81 write DRQ; wait for DOR and BCE = logic 1 or IRDR; P82 read <DATA>; (16 bytes); P81 write ETR; within 125 µs after the 16th byte is read from P82.
PCB2310 input initiated by microcontroller (> 16 bytes)	
a	P82 write (16 bytes) <CTRL>[<PAR>] [<DATA>] ; wait for DIR or IDIR, P82 write (next bytes) <DATA>; P81 write ETR.
b	P82 write (16 bytes) <CTRL>[<PAR>] [<DATA>] ; wait for DIR or IDIR, P82 write (next bytes) <DATA>; P81 write DRQ; wait for (DOR and BCE) or IRDR; P82 read (16 bytes) <DATA>; wait for (DOR and BCE) or IRDR; P82 read (next bytes) <DATA>; (16 bytes); P81 write ETR; within 125 µs after the 16th byte is read from P82.
PCB2310 output initiated internally (DOR = logic 1 and BCE = logic 0 or IDOR = logic 1)	
c	P82 read <CTRL>[<PAR>] [<DATA>] ; number of bytes written in NB2 to NB0.

Where:

<CTRL> = control command byte
<PAR> = one or more parameter byte(s)
<DATA> = one or more information byte(s)
[ ]   = optional

Table 2.6-6　Register P82; I/O control commands

MNEM.	OP. CODE <CTRL>	PARAMETER <PAR>	DATA [<DATA>]	MODE*	DESCRIPTION
					internal RAM/register read/write access
LOD	10	^1st address	n bytes	a	load data in RAM
LOR	11	^1st address	n bytes	a	load register RR
FED	12	^1st address	–	b	fetch data from RAM
FER	13	^1st address	–	b	fetch register
RST	00	–	–	a	soft reset and start**
					bd channel interface primitives
LSP	08	IST_DEA	[n bytes]	a	load 's' transmit buffer
LST	09	[IST_DEA]	[n bytes]	a	load 's' transmit buffer and transfer
LDP	0A	IST_DEA	[n bytes]	a	load 'd' transmit buffer
LDT	0B	[IST_DEA]	[n bytes]	a	load 'd' transmit buffer and transfer
TSC	0E	–	–	b	transfer 's' receive buffer to microcontroller
TDC	0F	–	–	b	transfer 'd' receive buffer to microcontroller
RSB	01	–	–	a	release 's' receive buffer
RDB	02	–	–	a	release 'd' receive buffer
SPR	31	–	3 bytes △	c	's' packet receive indication
DPR	32	–	3 bytes	c	'd' packet receive indication
SPT	33	–	–	c	's' packet transmit confirmation
DPT	34	–	–	c	'd' packet transmit confirmation
SPF	23	–	–	c	's' packet transfer failure indication
DPF	24	–	–	c	'd' packet transfer failure indication
					SLD channel control
SBS	18	TS	[TS]	a	SLD B channel/TSA selection
SCT	1A	–	[n bytes]	a or b	SLD C channel transfer
					circuit-switched channel selection
FFC	03	–	–	a	fetch free channel
OAR	0D	IST b1-8	–	a	occupy channel directly after release
RCH	0C	IST b1-8	–	a	release channel(s)
CHC	30	IST b1-8	–	c	channel has been connected

Table 2.6-6 (continued)

MNEM.	OP. CODE <CTRL>	PARAMETER <PAR>	DATA [<DATA>]	MODE*	DESCRIPTION
					master-slave arbitration/maintenance
FMF	22	–	–	c	FCM transfer failure indication
TRM	06	–	–	a	Transfer IST bus master
TMP	20	–	–	c	IST bus down
TMF	21	–	–	c	IST bus up
					external synchronization procedures
ESR	04	–	–	a	external synchronization request
RES	05	–	–	a	release external synchronization
ESO	25	–	–	c	external synchronization is on
ESW	26	–	–	c	external synchronization is required
RSP	27	–	–	c	release of external synchronization will proceed

Where:

[..]	=	optional
—	=	no parameter or data-bytes
*	=	modes a, b and c are as in Table 2.6-5
^1st address	=	pointer to first register/RAM address
IST_DEA	=	IST destination address. The message loaded in the PCB2310 will be transmitted in the bd channel and the IST destination address is transmitted in the control byte of the bd message. (see bd message format Table 2.8-1).
IST b1-8	=	The format of the parameter is as follows:

bit 7   0

b8	b7	b6	b5	b4	b3	b2	b1
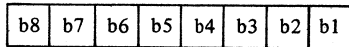
In the commands <OAR> and <RCH> a logic 1 in one or more specific bit position(s) indicates that the applicable channel(s) should be occupied then released. In the response <CHC> a logic 1 in the specific bit position indicates that the appropriate channel has been occupied. All logic 0's in the parameter indicates that all channels are occupied at the moment.

**	=	<RST> command is used for initialization.
Δ	=	see section 2.7.4; bd channel interface primitives.
TS	=	Up to four parameter bytes can be given. The format of the parameter is as follows:

bit 7   0

c	c	c	c	c	d	b	b
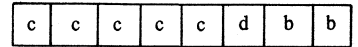
ccccc = the 5-bit binary decoding of the THW_slot_nr

If TSA = LOW the <SBS> command controls the SLD switch and programs the strobe outputs RX2 and TX2

d = 0   SIP output is inactive
        SLD slave: 3-state
        SLD master: all logic 1's
        THW output is active

d = 1   SIP output is active
        THW output is inactive (3-state)

bb = 00   THW time slot ccccc is switched to B_1 SLD

bb = 01   THW time slot ccccc is switched to B_2 SLD
          strobe signal RX2 (pin 11) falls over THW time slot ccccc

bb = 10 B_1 SLD is switched to THW time slot ccccc (d = don' t care)

bb = 11 B_2 SLD is switched to THW time slot ccccc
          strobe signal TX2 (pin 17) falls over THW time slot ccccc

If TSA = HIGH the <SBS> command programs the strobe outputs

d = don't care

bb = 00   strobe signal RX1 (pin 13) falls over THW time slot ccccc

bb = 01   strobe signal RX2 (pin 11) falls over THW time slot ccccc

bb = 10   strobe signal TX1 (pin 16) falls over THW time slot ccccc

bb = 11   strobe signal TX2 (pin 17) falls over THW time slot ccccc.

2.7 Command description

2.7.1 Internal RAM/register read/write access

Commands to access the internal 256 x 8 RAM:

- <FED> to READ
- <LOD> to WRITE

Commands to access the internal registers:

- <FER> to READ
- <LOR> to WRITE

Care must be taken when writing to RAM and register locations otherwise it may cause unwanted actions.

Table 2.7-1 RAM allocation map

ADDR. HEX.	CONTENTS OF LOCATION
00 01 02	for internal use — IST bus address*
03 .. .. 0E	these RAM byte locations are for internal use and are not allowed to be accessed by the user
0F	pointer to first address of 'd' transmit buffer**
10	pointer to first address of 's' receive buffer
11	pointer to first address of 'd' receive buffer
12 .. 1F	these RAM byte locations are for internal use and are not allowed to be accessed by the user
20 ..	's' transmit buffer
.. ..	'd' transmit buffer
.. ..	's' receiver buffer
.. FF	'd' receive buffer

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Where:

* The IST bus, 5-bit binary coded address, should be loaded at initialization by the user.

bit 7   0

xxx IST addr
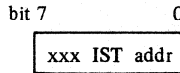
Each member on the IST bus should have a different address. If an addressed packet is transmitted on the bd channel the packet will be loaded by the PCB2310 whose IST bus address is equal to the DEA address (see Table 2.7-1). Broadcast messages will be loaded by all PCB2310s connected to the IST bus.

** The user allocates the buffer pointers by initialization (see <RST> command Table 2.6-6).

<command><pointer>[<data>]	**pointer →**	data_byte 1
		data_byte 2
		data_byte n

Initially the pointer is equal to <pointer>. Each time a new <data> is written/read the pointer is incremented.

Fig. 2.7-1 Internal RAM/register read/write access.
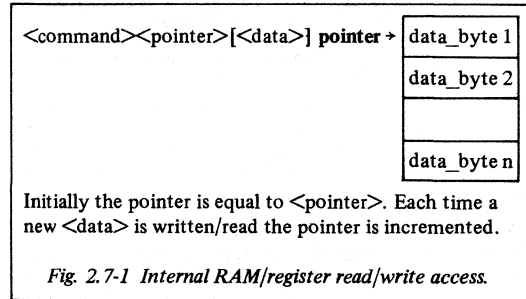
2.7.2 Registers

The address map of the internal PCB2310 registers and data bus I/O ports is shown by Table 2.7-2. The addresses are the access codes to input or output a byte to or from the internal data bus.

Table 2.7-2 Register allocation

ADDR.	PURPOSE OF THE ADDRESS	REMARKS
06	bit 2 = monitor mode bit*	see section 2.10
	bit 3 = external sync on	8 kHz on pin 13 (ESC and VSL)
0D	enable b1 to b8	transmit in b1 to b8 channel
0E	occupied b1 to b8	start bit b1 to b8 channel detected
0F	bit 2 = any signal on IST	signal detected on IST bus
	bit 5 = VSL	VSL (pin 8 = HIGH)
	bit 6 = lock	locked to F channel (8 kHz)
	bit 7 = master/enable frame	transmit in F channel

*The monitor mode can be chosen with

R6old = <FER><06>(read old contents of register 06)
R6new = R6old or 04 (bitwise OR of old value with 04)
<LOR><06><R6new>(write new contents into register 06)

Be aware that the <RST> command also resets the THW monitor mode.

Note: The user is not allowed to set the registers.
Addresses not mentioned are for internal use only.

2.7.3 Reset command

After RESET (pin 7) goes LOW (internally or externally activated; see section 2.9) a chip 'wait state' follows. In this event the IST bus address must be loaded at RAM location hex 02 using command <LOD> and the pointers to the first addresses of the various packet buffers must be loaded in RAM address hex 0F-11 (see Table 2.7-1). After reception of the command <RST> the PCB2310 enters the normal operating mode.

<LOD> and <RST> command the start up operation of PCB2310.

- 1st command : <LOD><02><IBA>
- 2nd command: <LOD><0F><--><--><-->
- 3rd command : <RST>

If the <RST> command is received during normal operation, provided the PCB2310 is an IST slave terminal and a gateway station (VSL = logic 1), it will transmit a TOM Frame Control message in the bd channel. An inhibited IST master function will be reset (see section 2.7.7; master-slave control), also the b1 to b8 channels and the 's' and 'd' receive and transmit buffers will be released.

2.7.4 bd channel interface primitives

Transmit

To transmit 's' or 'd' type messages the following four primitives are used:

- <LSP>; <LST>:
  <'s'_type_transmission_request><<data>>
- <LDP>; <LDT>:
  <'d'_type_transmission_request><<data>>

With command <LST> the 's' transmit buffer is loaded and transmitted in the bd channel.
With command <LDT> the 'd' transmit buffer is loaded and transmitted in the bd channel.
The first data byte in these buffers is used as the IST destination address in the bd message control field.
At the end of the message transfer two CRC bytes are added by the PCB2310.

With command <LSP> an 's' type message could be loaded in the 's' transmit buffer without being transmitted.
With command <LDP> a 'd' type message could be loaded in the 'd' transmit buffer without being transmitted.
The information stored in the 's' and 'd' buffers can then be transmitted with additional data bytes, if required, by commands <LST>, <LDT> respectively.

Note:

The first byte loaded by commands <LSP>, <LDP> is used as the IST destination address.

Data stored in these buffers is held until new data is loaded. Thus it is possible to re-transmit previously stored messages by command <LST> or <LDT> without the requirement for additional data bytes.

If an 's' or 'd' packet is transferred correctly an <SPT> or <DPT> transfer_confirmation primitive is given.

If an 's' or 'd' type message could not be transferred correctly an <SPF> or <DPF> error primitive is issued.

If after four internally generated re-transmissions $\overline{ACK}$ is still received (see IST bus specification) this indicates that a message could not be transferred correctly.
If an internal frame control message could not be transferred correctly an <FMF> primitive is issued (see IST bus specification and section 2.8 bd channel protocol).

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Receive

When an 's' or 'd' type packet is received correctly the PCB2310 initiates a message received primitive:

- <SPR>: <'s' message received primitive><<data>>
- <DPR>: <'d' message received primitive><<data>>

The 3 data bytes that follow these <SPR>, <DPR> primitives indicate:

- 1st byte : pointer to (last address + 1) of packet loaded in RAM
- 2nd byte: first byte of received packet
- 3rd byte : second byte of received packet

With commands <TSC>, <TDC> the received packet, minus first two bytes of the received packet, is transferred to the microcontroller (first two bytes of the packet will not be transmitted again). The number of bytes to be fetched is:

(1st byte received after <SPR>, <DPR> command) − (pointer_to_first_buffer location) − 2.

Provided 's' or 'd' receive buffers are not released with command <RSB> or <RDB>, the PCB2310 will be blocked to receive any further message of the type of held in the filled buffer. The PCB2310 will now transmit an $\overline{ACK}$ on the IST bus. In effect this is flow control.

2.7.5 SLD channel control

The SLD S channel is 'quasi transparent' through the PCB2310 and is controlled directly via register P83 on the microcontroller port. Transmit and receive status bits SST and SSR can be polled in P81, or can generate an IREQ (see Table 2.6-4).

The B_1 and B_2 channels are controlled by command <SBS> and the C channel by command <SCT>.

The <SBS> command can be used in both SLD master mode and SLD slave mode. The <SCT> command is only effective in the SLD master mode.

The <SBS> command writes directly to one or more registers that control the SLD/THW switch. Channels b1 to b8 on the IST bus are mapped upon time slots on the THW and from then on can be switched to the SLD B channels and vice versa.

In the TSA mode the <SBS> command data bytes determine the THW time slot strobe signals.

Following the <SCT> command data bytes are transferred in the SLD C channel. If there are no data bytes to be transmitted an NOP code (hex FF) is transmitted in the SLD master mode. If data is expected in return on the SLD C' channel the <SCT> command should be ended by writing the DRQ bit instead of ETR bit in P81. Bits DOR and BCE in the polling mode, or IRDR when in the interrupt mode, indicates that 16 bytes received on the SLD C' channel have been loaded in the P82 FIFO. The maximum number of bytes that can be returned to this channel is 16.

2.7.6 Circuit-switched channel control (IST b1 to b8)

With command <FFC> a free IST b channel will be occupied. If a channel has been occupied, the PCB2310 issues a <CHC> primitive; the parameter following this command indicates which channel has been occupied. If there is no free channel the parameter following <CHC> is hex 00. The data on the corresponding THW time slot will be transmitted in the occupied IST b channel (see Fig. 2.4-1). The b channel access protocol guarantees a unique channel allocation.

With the command <RCH> followed by a parameter the indicated IST b channel will be released. If the parameter is hex FF all channels occupied by the PCB2310 will be released.

With the <OAR> command* followed by a parameter indicating an IST b channel, that specific channel will be occupied immediately after it has been released. If the channel has been occupied a <CHC> primitive will be issued. This makes it possible to transfer IST b channel control from one PCB2310 to another. It is not allowed to perform the <OAR> command on two or more PCB2310s at the same time with the same IST b channel parameter.

* If an <OAR> command is issued the PCB2310 will wait until that specific channel has been released. An <FFC> command must never be given before the <OAR> command has been completed by receiving a <CHC> confirmation.

2.7.7 IST master-slave control/maintenance commands

The complete master-slave protocol as prescribed in the IST bus specification is implemented in the PCB2310. The PCB2310 initiates a data output request if there is no signal on the IST bus for at least one IST frame (125 μs). The command sent is <TMP>. When there is a signal on the IST bus the command <TMF> will be issued.

If a terminal wants to disconnect from the IST bus lines it has to issue a <TRM> command to the PCB2310. If the PCB2310 responds with a <TMP> primitive followed by <TMF>, or only <TMF>, the terminal is allowed to disconnect from the IST bus. The PCB2310, if IST master, will cease transmission in the frame channel as soon as all circuit-switched IST b1 to b8 channels are free. The master slave arbitration procedure will start again but the PCB2310 that received the <TRM> is not allowed to participate in this procedure, however all other I/O commands can still be entered into that PCB2310. To allow the PCB2310 to participate again an <RST> command should be entered.

2.7.8 External synchronization procedures

These procedures are used to synchronize the IST bus to an external network connected via a gateway. They also incorporate additional PCB2310s on the same IST bus being connected to an external network.

With <ESR> command the microcontroller, via the PCB2310, requests the IST bus to synchronize to an 8 kHz external source. The PCB2310 that is IST master will issue an <ESW> primitive which indicates to the microcontroller that external synchronization is requested. If the master detects an 8 kHz signal on ESC/SDIR (pin 14) and VSL (pin 8) is HIGH, the master sends the control message <SCO> on the IST bus (see IST bus specification). All PCB2310s then give an <ESO> primitive.

Once external synchronization is established terminals can communicate via the gateway to other networks.

To terminate the external synchronization an <RES> request should be entered in the PCB2310. All slave terminals will give an <RSP> primitive. If no <ESR> command is given within 8 seconds, the gateway also gives an <RSP> primitive and the microcontroller can now release the external synchronization.

2.8 bd channel protocol

The PCB2310 implements full layer 1 and 2 protocol as described in the IST bus specification. The service access point of the layer 2 entity is register P82 FIFO (see section 2.7.4 bd channel interface primitives). If the THW is in monitor mode the bd channel receiver information is mapped to the THW time slot 7 for test purposes.

Features of the bd channel layer 2 functions

- Packet-switched transmission
- Specific destination or broadcast address
- Access via microcontroller I/O port
- Error detection/correction by re-transmission
- Flow control
- Byte oriented
- Fully transparant for layer 3 messages

Table 2.8-1 bd channel message format

MESSAGE	DESCRIPTION
1	<I , s, DEA><<DATA>> <CRC><CRC><EMPT><$\overline{ACK}$>
2	<I , d, DEA><<DATA>> <CRC><CRC><EMPT><$\overline{ACK}$>
3	<C, FCM> <CRC><CRC><EMPT><$\overline{ACK}$>

Where:

< >	=	byte
<< >>	=	0 to n bytes
DEA	=	5-bit destination address (logic 0 = broadcast). DEA is the 5 least significant bits of the first byte loaded in the 's' or 'd' buffer. (see Table 2.6-5; <LST> and <LDT>)
DATA	=	data octets
CRC	=	first and second octet of the CRC word
EMPT	=	empty bd channel during one frame (no start and data bits)
$\overline{ACK}$	=	not acknowledge code (11111111)
FCM	=	frame control message
I	=	information mode (I = logic 0)
C	=	link control mode (C = logic 1)
s	=	signalling packet (s = logic 1)
d	=	data packet (d = logic 0)

2.8.1 bd channel access protocol

The bd channel access protocol makes use of the Carrier Sense Multi-Access principle with Collision Detection (CSMA/CD). Some extra features have been added which guarantee full accessability under high traffic circumstances, and give signalling messages, loaded in the 's' transmit buffer, priority over waiting data packets loaded in the 'd' transmit buffer (see Table 2.6-6; <LST> and <LDT>).

To shorten the average bus occupation time during collisions, an 'exclusive OR' function has been implemented between the bus transmitter and receiver. This facilitates immediate collision detection by not having to wait for CRC errors at the end of the complete transport. The AMI line code uses the +1 and −1 polarity to transmit a logic 1 on the bus. A logic 0 is transmitted as a floating bus potential

which will be overridden by a logic 1.

A transmitting station can detect this situation by comparing its output with the receiver signal. A collision detected in this way is serviced by transmitting the all logic 1's code in the next frame and then stops transmission. The other stations now have the possibility of detecting the collision and immediately stop transmissions. All stations transmit the $\overline{ACK}$ code in the N frame and re-transmissions can start by the previously described protocol.

2.9 Reset (see Fig. 2.9-1)

The PCB2310 internal reset circuit will be activated when V_{DD1} is below 1,2 V and rising to 5 V with a slope greater than 5 V/ms and connected to $\overline{PO}$ (pin 4). It is also possible to reset the PCB2310 externally by a pulse of $> 1\ \mu s$ being applied to $\overline{PO}$ (active LOW). After reset the PCB2310 initializes all register and RAM locations to zero. At this time the RESET output (pin 7) is active HIGH. This output is used to reset other circuits such as the microcontroller. After pin 7 goes LOW again the PCB2310 expects data to be filled in the RAM followed by the <RST> command (see section 2.7.3; reset command). After reception of the command <RST> the PCB2310 is initialized and enters the normal operating mode. There is no power down mode.

2.10 Monitor mode

The circuit has a built-in mode for monitoring the bd channel. Monitor mode is selected with address RR06 bit 2 (see Table 2.7-2). In this mode the THSC sync pulse has two states:

- Idle bd channel
  THSC pulse has a 1-bit duration and falls over bit 0 of time slot 6
- Busy bd channel
  THSC pulse has a 9-bit duration and falls over bit 0 of time slot 6 and bit 7 to 0 of time slot 7.

2.11 Crystal connection circuit (see Fig. 2.11-1)

One side of the crystal is connected to pin 1. When using an external clock generator pin 1 is not connected. The other side of the crystal is connected to pin 3. An 8192 kHz $\pm 100 \times 10^{-6}$ crystal with $C_L = 20$ pF must be used. An external clock generator can also be connected to pin 3.

The PCB2310 has a Pierce oscillator (Fig. 2.11-2) oscillating on a frequency f_1, where

$$f_1 = \frac{1}{2\pi \sqrt{L_1 \cdot \dfrac{C_1 (C_0 + C_L)}{C_1 + C_0 + C_L}}}$$

Values for the crystal are:

$f_1 = 8192$ kHz $\pm 100 \times 10^{-6}$

$C_0 = 5.1$ pF $\pm 20\%$

$C_1 = 21.5$ fF $\pm 20\%$

$R_1 = 60\ \Omega$

Level of drive = 0.5 mW (a 1 kΩ resistor in series with the crystal limits the level of drive to 0.5 mW).

$C_L = 20$ pF

$= \dfrac{C_{L1} (C_{L2} + C_{ext})}{C_{L1} + C_{L2} + C_{ext}}$
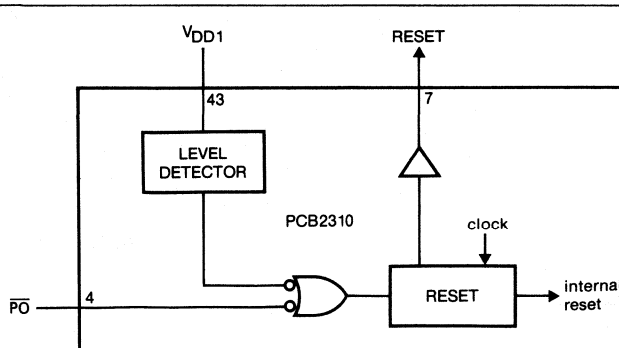
Fig. 2.9-1 Reset circuit (simplified).   7Z81410.1

Fig. 2.11-1 Crystal connection.

Fig. 2.11-2 Crystal definitions.
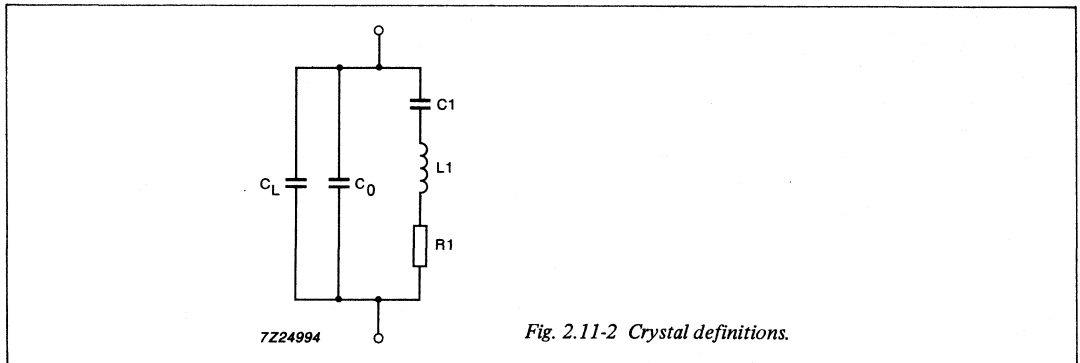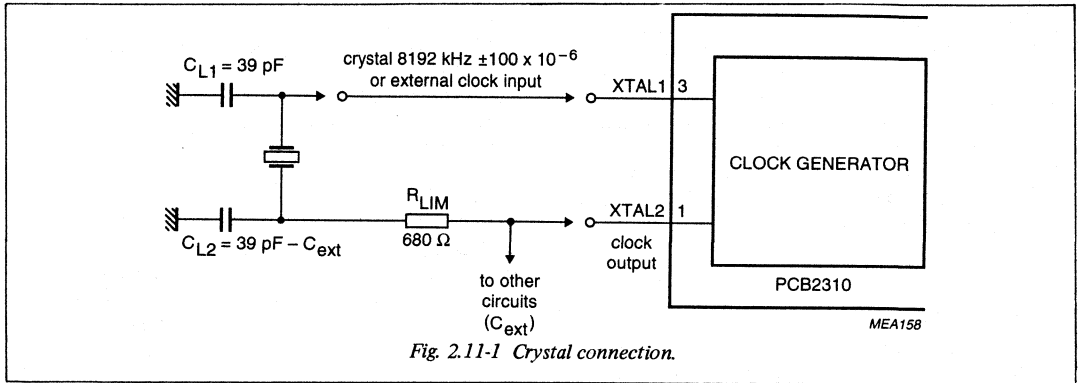
3.0 ELECTRICAL SPECIFICATION

3.1 Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages are referenced to GND (ground = 0 V)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	$-0,5$	$7,0$	V
DC input diode current	$V_I < -0,5$ V or $V_I > V_{DD} +0,5$ V	$\pm I_{IK}$	$-$	10	mA
DC output diode current	$V_O < -0,5$ V or $V_O > V_{DD} +0,5$ V	$\pm I_{OK}$	$-$	10	mA
DC output source or sink current	$-0,5$ V $< V_O < V_{DD} +0,5$ V	$\pm I_O$	$-$	10	mA
DC V_{DD} current		$\pm I_{DD}$	$-$	50	mA
DC GND current		$\pm I_{GND}$	$-$	50	mA
Voltage on any pin		V_n	0	V_{DD}	V
Storage temperature range		T_{stg}	-65	$+150$	°C
Operating ambient temperature range		T_{amb}	0	$+70$	°C
Total power dissipation	temperature range: 0 to +70 °C above +70 °C: derate linearly with 8 mW/K	P_{tot}	$-$	500	mW

3.2 DC Characteristics

V_{DD} = 5 V nominal; T_{amb} = 25 °C; unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC supply voltage						
analogue	note 1	V_{DD1}	4,75	5,0	5,25	V
digital	note 2	V_{DD2}	4,75	5,0	5,25	V
Average operating current						
analogue		I_{DD1}	–	2,0	–	mA
digital		I_{DD2}	–	15,0	–	mA
Quiescent current	note 3					
analogue		I_{DD1}	–	–	1,0	mA
digital	T_{amb} = 25 °C	I_{DD2}	–	–	100	μA
Inputs						
Input voltage LOW						
all inputs except $\overline{PO}$; XTAL1; ISTIN	V_{DD} = 4,75 V	V_{IL}	–	< 0.5	–	V
Input voltage LOW $\overline{PO}$	V_{DD} = 4,75 V	V_{IL}	–	< 1.4	–	V
Input voltage LOW XTAL1	V_{DD} = 4,75 V	V_{IL}	–	< 2	–	V
Input voltage HIGH						
all inputs except $\overline{PO}$; XTAL1; ISTIN	V_{DD} = 5,25 V	V_{IH}	–	> 1.9	–	V
Input voltage HIGH $\overline{PO}$	V_{DD} = 5,25 V	V_{IH}	–	> 3.2	–	V
Input voltage HIGH XTAL1	V_{DD} = 5,25 V	V_{IH}	–	> 3	–	V
ISTIN input voltage						
positive pulse		V_{IP}	ISTREF+0,7	–	–	V
zero level		V_{IZ}	ISTREF−0,5	–	ISTREF+0,5	V
negative pulse		V_{IN}	–	–	ISTREF−0,7	V
Input leakage current	T_{amb} = 25 °C; V_I = V_{DD} to 0 V	I_{IL}	−1	–	+1	μA
Outputs						
Output voltage LOW						
all outputs	I_{OL} = 20 μA	V_{OL}	–	< 0.05	–	V
Output voltage LOW						
all outputs except THCL; XTAL2; ISTOUT1; ISTOUT2; ISTREF	I_{OL} = 3 mA	V_{OL}	–	–	0,3	V
Output voltage LOW THCL	I_{OL} = 6 mA	V_{OL}	–	–	0,3	V
Output voltage LOW XTAL 2	I_{OL} = 0,7 mA	V_{OL}	–	–	0,6	V
Output voltage LOW ISTOUT1; ISTOUT2	I_{OL} = 7.5 mA	V_{OL}	–	–	2,4	V
Output voltage HIGH						
all outputs	$-I_{OH}$ = 20 μA	V_{OH}	–	> V_{DD2} −0.05	–	V
Output voltage HIGH						
all outputs except THCL; XTAL2; $\overline{IREQ}$; ISTOUT1; ISTOUT2; ISTREF	note 4; $-I_{OH}$ = 3 mA	V_{OH}	V_{DD2}−0,3	–	–	V
Output voltage HIGH THCL	$-I_{OH}$ = 6 mA	V_{OH}	V_{DD2}−0,3	–	–	V
Output voltage HIGH XTAL2	$-I_{OH}$ = 0,6 mA	V_{OH}	V_{DD2}−0,5	–	–	V
Output voltage HIGH ISTOUT1; ISTOUT2	$-I_{OH}$ = 7.5 mA	V_{OH}	V_{DD2}−2,1	–	–	V
Output voltage ISTREF		V_{REF}	$\frac{V_{DD1}}{2}$−0,06	–	$\frac{V_{DD1}}{2}$+0,06	V
3-state OFF current	T_{amb} = 25 °C	$\pm I_{OZ}$	–	–	5	μA

Notes to DC characteristics

1. Noise on the analogue supply voltage V_{DD1} must be less than 25 mV for frequencies above 1 kHz.
2. All IST b1 to b8 channels occupied.
3. The input pins must have the following conditions:
   V_I = V_{SS} for pins 4, 8, 9, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 25, 26, 27, 32, 35, 36, 37, 41;
   V_I = V_{DD} for pins 13, 30, 31, 33, 38, 39, 43, 44;
   all other pins are not connected;
   pin 3 must receive at least 25 clock cycles before it is connected to V_{SS}.
4. $\overline{IREQ}$ is an open drain NMOS output.

DEVELOPMENT DATA

3.2.1 Capacitance

V_{SS} = GND = 0 V; T_{amb} = +25 °C

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	f = 1 MHz	C_I	–	–	5	pF
Input/output capacitance		$C_{I/O}$	–	–	20	pF
Output capacitance	other outputs to GND	C_O	–	–	15	pF

3.3 AC Characteristics

V_{DD} = 5 V nominal; T_{amb} = 25 °C, unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Terminal Highway (Fig. 3.3-1)	C_L = 150 pF note 1					
THCL						
clock period	note 2	t_W	–	$(4f_{XTAL1})^{-1}$	–	ns
duty factor	note 2	t_{WH}/t_W	–	50	–	%
THDA output propagation delay THCL to THDA						
in master mode		t_{PHL}, t_{PLH}	–	<75	–	ns
in slave mode		t_{PHL}, t_{PLH}	–	<350	–	ns
3-state output disable						
in master mode		t_{PHZ}, t_{PLZ}	–	<80	–	ns
in slave mode		t_{PHZ}, t_{PLZ}	–	<80	–	ns
THDA input set-up time THDA to THCL						
in master mode		t_{su}	–	>75	–	ns
in slave mode	note 3	t_{su}	–	>−195	–	ns
hold time THDA to THCL		t_h	–	>−200		ns
in master mode		t_h	–	>230	–	ns
in slave mode	note 3	t_h	–	>320	–	ns
THSC output propagation delay THCL to THSC		t_{PHL}, t_{PLH}	–	–	75	ns
THSC input						
set-up time THSC to THCL		t_{su}	–	>−200	–	ns
hold time THSC to THCL		t_h	–	>320	–	ns
TX1, TX2, RX1, RX2 propagation delay THCL to TX, RX						
in master mode		t_{PHL}, t_{PLH}	–	<75	–	ns
in slave mode	note 3	t_{PHL}, t_{PLH}	–	<350	–	ns
All outputs output transition time		t_{THL}, t_{TLH}	–	<50	–	ns

3.3 AC Characteristics (continued)

PARAMETER	CONDITONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
SLD bus (Fig. 3.3-2)	$C_L = 150\,pF$					
SCLK						
clock period	note 2	t_W	—	$(16f_{XTAL1})^{-1}$	—	ns
duty factor	note 2	t_{WH}/t_W	—	50	—	%
SIP output						
propagation delay SCLK to SIP						
in master mode		t_{PHL},t_{PLH}	—	<75	—	ns
in slave mode		t_{PHL},t_{PLH}	—	<75	—	ns
disable time SCLK to SIP						
in master mode		t_{PHZ},t_{PLZ}	—	<80	—	ns
in slave mode		t_{PHZ},t_{PLZ}	—	<80	—	ns
SIP input						
set-up time SIP to SCLK						
in master mode		t_{su}	—	>-640	—	ns
in slave mode		t_{su}	—	>75	—	ns
hold time SIP to SCLK						
in master mode		t_h	—	>990	—	ns
in slave mode		t_h	—	>75	—	ns
SDIR output						
propagation delay SCLK to SDIR		t_{PHL},t_{PLH}	—	>0	—	ns
SDIR input						
set-up time SDIR to SCLK		t_{su}	—	>75	—	ns
All outputs						
output transition time		t_{THL},t_{TLH}	—	<50	—	ns

3.3 AC Characteristics (continued)

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Microcontroller bus (Fig. 3.3-3)	$C_L = 100$ pF					
ALE pulse duration		t_{LL}	–	> 100	–	ns
Address to ALE set-up time		t_{AL}	–	> 20	–	ns
Address hold time after ALE		t_{LA}	–	> 20	–	ns
$\overline{RD}$ pulse duration		t_{RR}	–	> 100	–	ns
$\overline{WR}$ pulse duration		t_{WW}	–	> 100	–	ns
Data delay time from $\overline{RD}$		t_{RD}	–	< 100	–	ns
Data hold time after $\overline{RD}$		t_{DR}	–	> 50	–	ns
Data float delay after $\overline{RD}$		t_{DFR}	–	< 95	–	ns
Time from ALE to $\overline{RD}, \overline{WR}$		t_{LW}	–	> 50	–	ns
Time from address to $\overline{RD}, \overline{WR}$		t_{AW}	–	> 20	–	ns
Time from $\overline{RD}, \overline{WR}$ HIGH to ALE HIGH		t_{WHLH}	–	> 20	–	ns
Data valid to $\overline{WR}$ transition		t_{DWX}	–	> 0	–	ns
Data set-up time before $\overline{WR}$		t_{DW}	–	> 100	–	ns
Data hold time after $\overline{WR}$		t_{WD}	–	> 20	–	ns
Address float delay after $\overline{RD}$		t_{AFR}	–	< 50	–	ns
IST bus I/O						
Output impedance		Z_O	–	5	–	kΩ
Pulse unbalance	note 4; $I_{OL} = 5$ mA; $-I_{OL} = 5$ mA	P_U	–	–	5	%

Notes to AC Characteristics

1. During a search for the frame word on the IST bus (LOCK bit 0F.6 is LOW) bit 5 of THW time slot 11 will be stretched with two THCL cycles.
2. PCB2310 uses terminal highway time slots 0 and 31 to synchronize to external sources. In these time slots the THCL clock period (t_W) can vary from −25% to +75%, the duty factor then varies from 67% to 72%. In these time slots SCLK clock periods can vary from −25% to +19%, the duty factor then varies from 31% to 58%.
3. If THW slave, the 8192 kHz clock of the THW master must be connected to XTAL2 (pin 1) of the slave. THCL from master to slave can be inverted when t_{HD} times are not reached.
4. Pulse unbalance (P_U), the relative difference between $\int U(t).dt$ for positive pulses and $\int U(t).dt$ for negative pulses, shall be $\leqslant$ 5%.

3.3.1 Timing
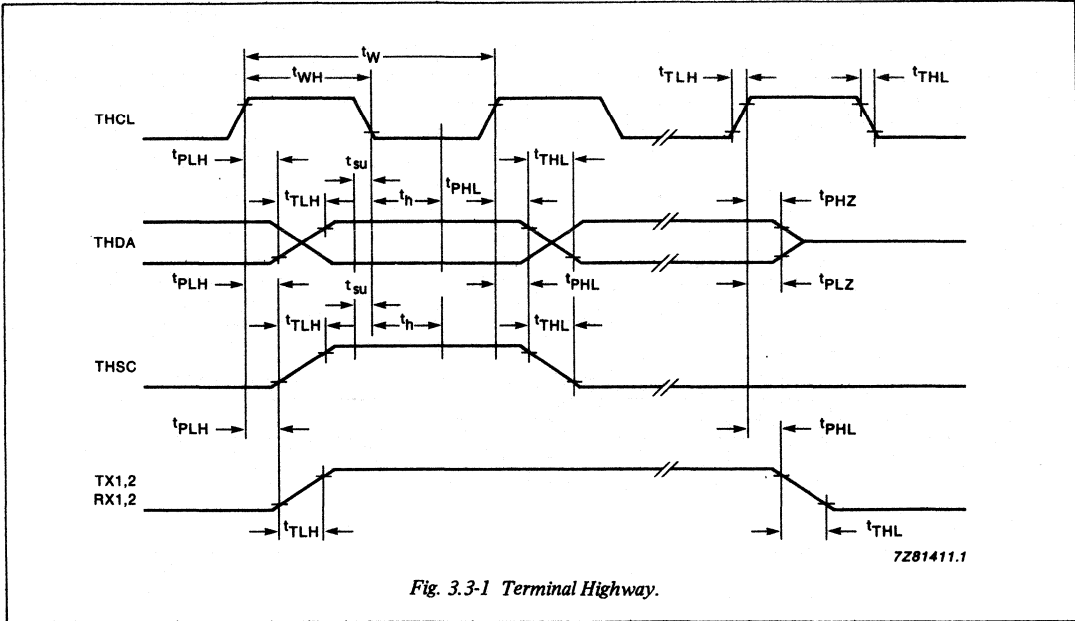
Fig. 3.3-1 Terminal Highway.
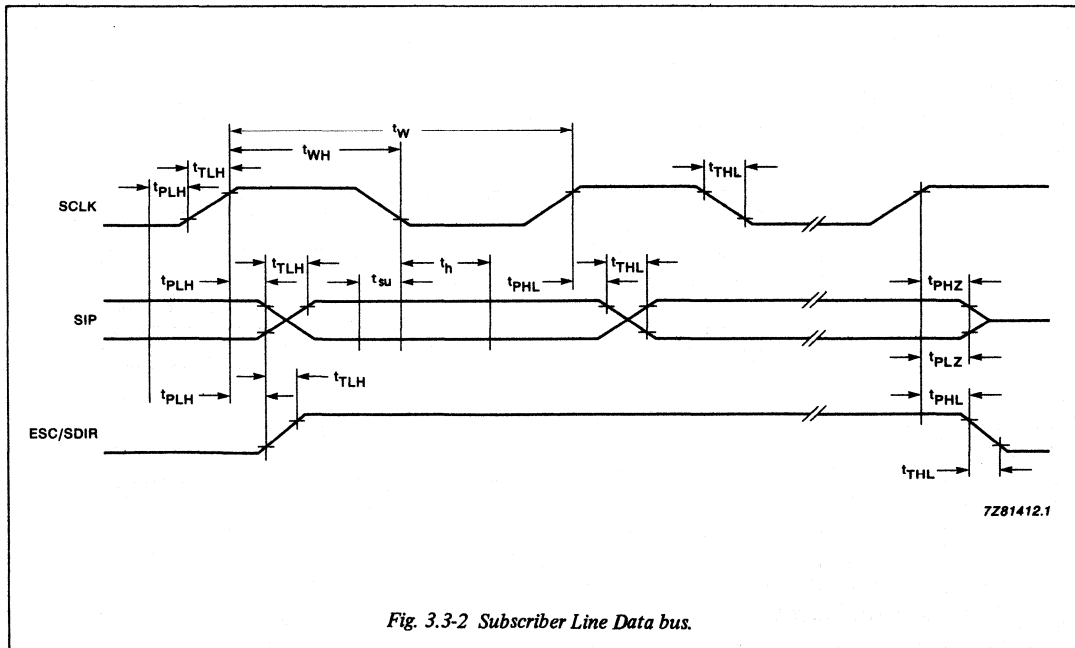
DEVELOPMENT DATA

Fig. 3.3-2 Subscriber Line Data bus.

Fig. 3.3-3 Microcontroller bus; (a) read from PCB2310 data memory; (b) write to PCB2310 data memory.

3.4 AC testing

Definitions:

$$V_1 = 0{,}5(V_{IL} + V_{IH})$$
$$V_2 = V_{OH} - 0{,}1(V_{OH} - V_{OL})$$
$$V_3 = V_{OL} + 0{,}1(V_{OH} - V_{OL})$$
$$V_4 = V_{OH} - 0{,}1(V_{OH} - V_{HZ})$$
$$V_5 = V_{HZ} + 0{,}1(V_{OH} - V_{HZ})$$
$$V_6 = V_{HZ} - 0{,}1(V_{HZ} - V_{OL})$$
$$V_7 = V_{OL} + 0{,}1(V_{HZ} - V_{OL})$$

(see DC characteristics for values of V_{IH}, V_{IL}, V_{OH} and V_{OL})

7Z24996.1
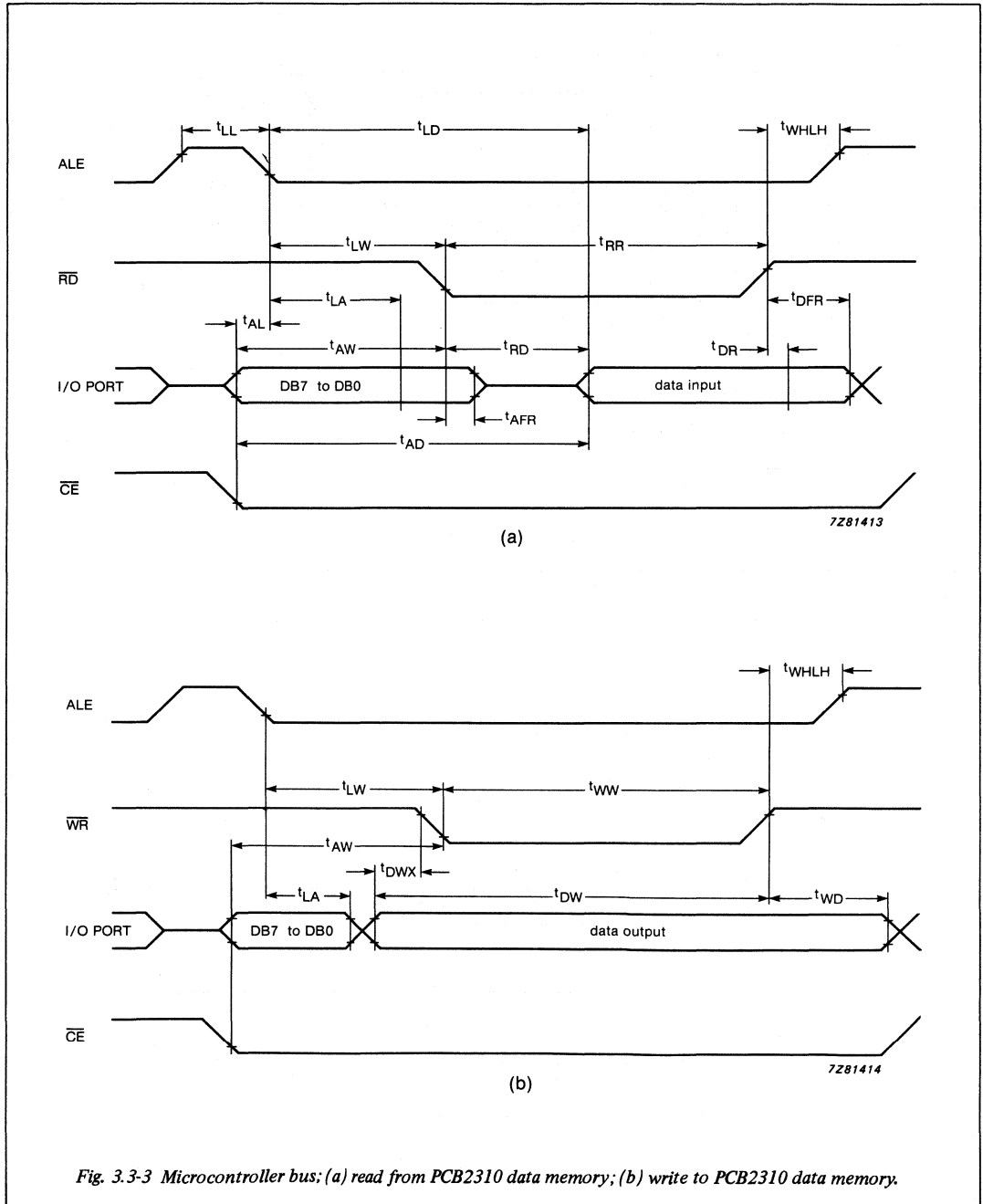
Fig. 3.4-1 Input, output and 3-state waveforms for AC testing.

DEVELOPMENT DATA

7Z24995

Definitions:

C_L load capacitance including jig and probe capacitance
          (see AC characteristics for values).

R_T termination resistance should be equal to the output
          impedance Z_O of the pulse generator.
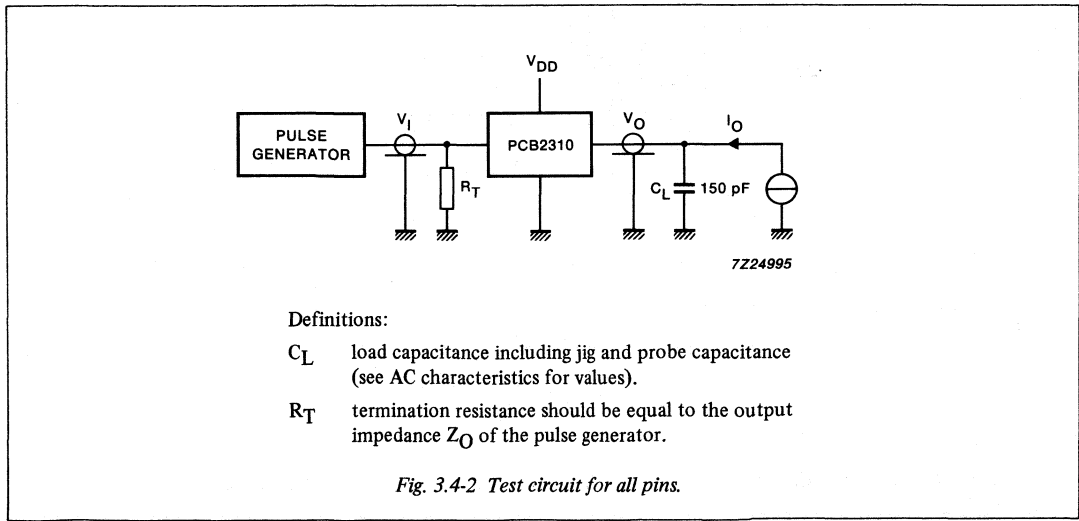
Fig. 3.4-2 Test circuit for all pins.

4.0 APPLICATION INFORMATION
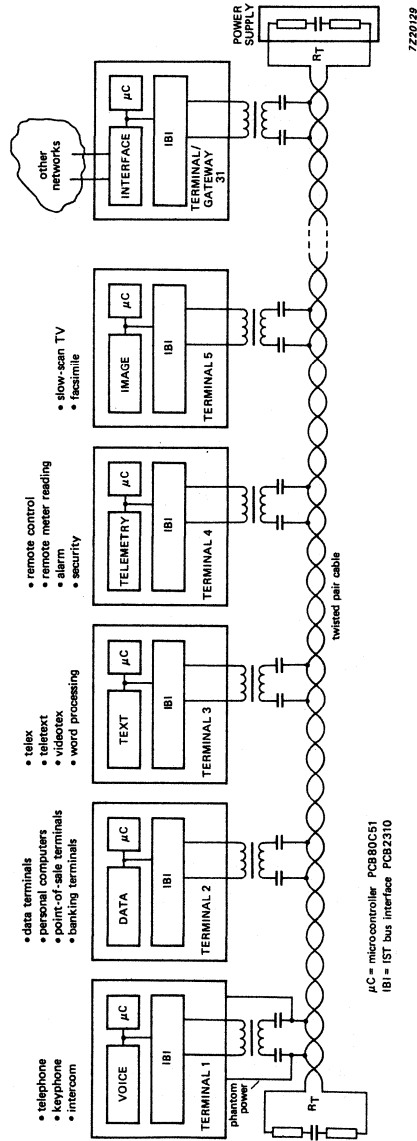
Fig. 4.0-1 IST bus configuration.
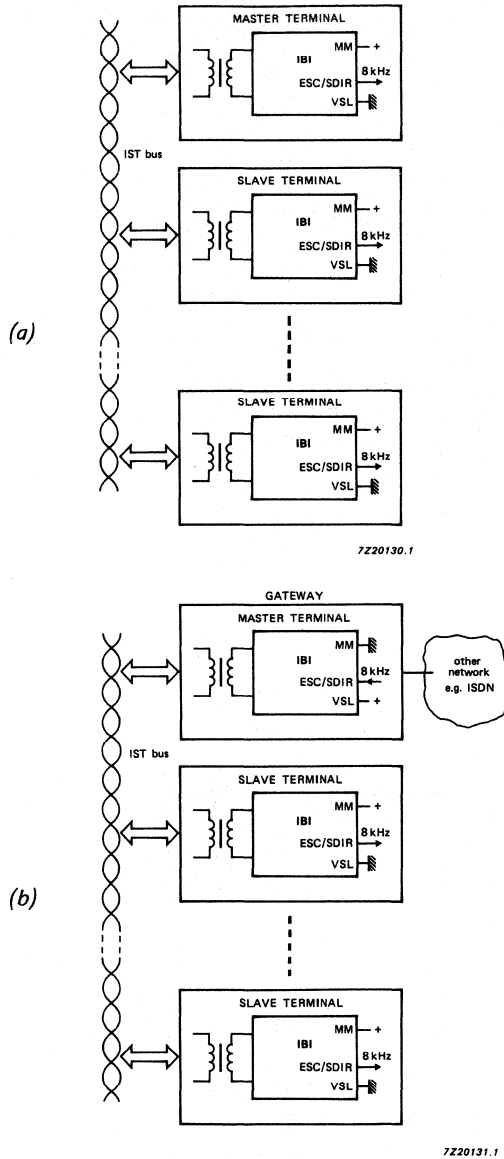
DEVELOPMENT DATA

Fig. 4.0-2 IST bus networks: (a) stand alone;
(b) with one gateway/gateway terminal.

(c)
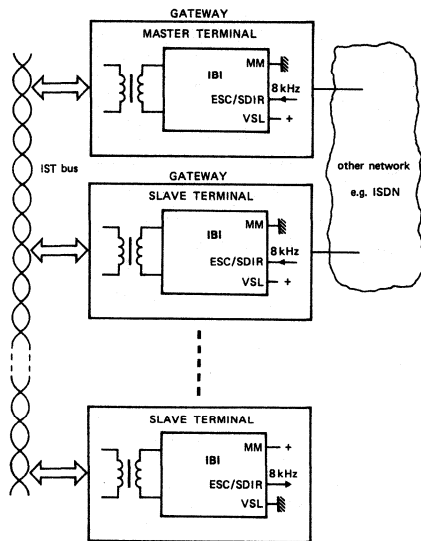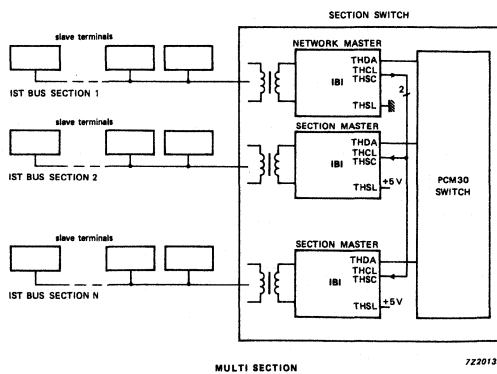
(d)

Fig. 4.0-2 IST bus networks: (c) with two or more gateways/terminals.
(d) multi section.

DEVELOPMENT DATA
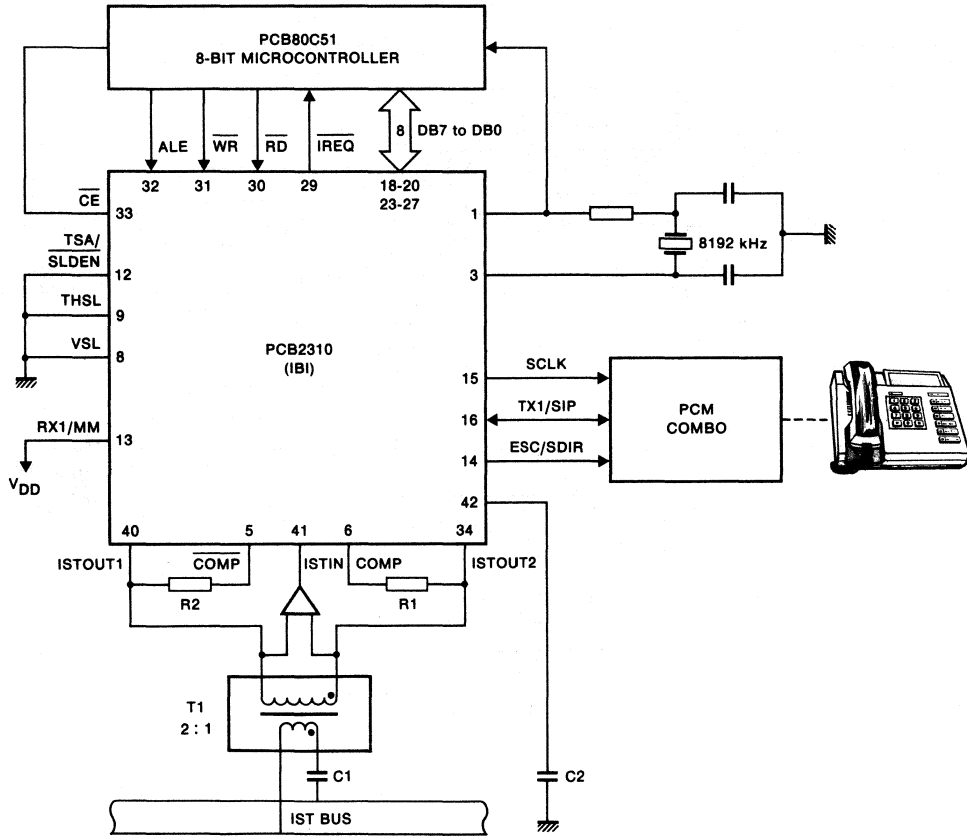
Fig. 4.0-3 Voice terminal: THW master mode; SLD master mode.

7Z81418.2
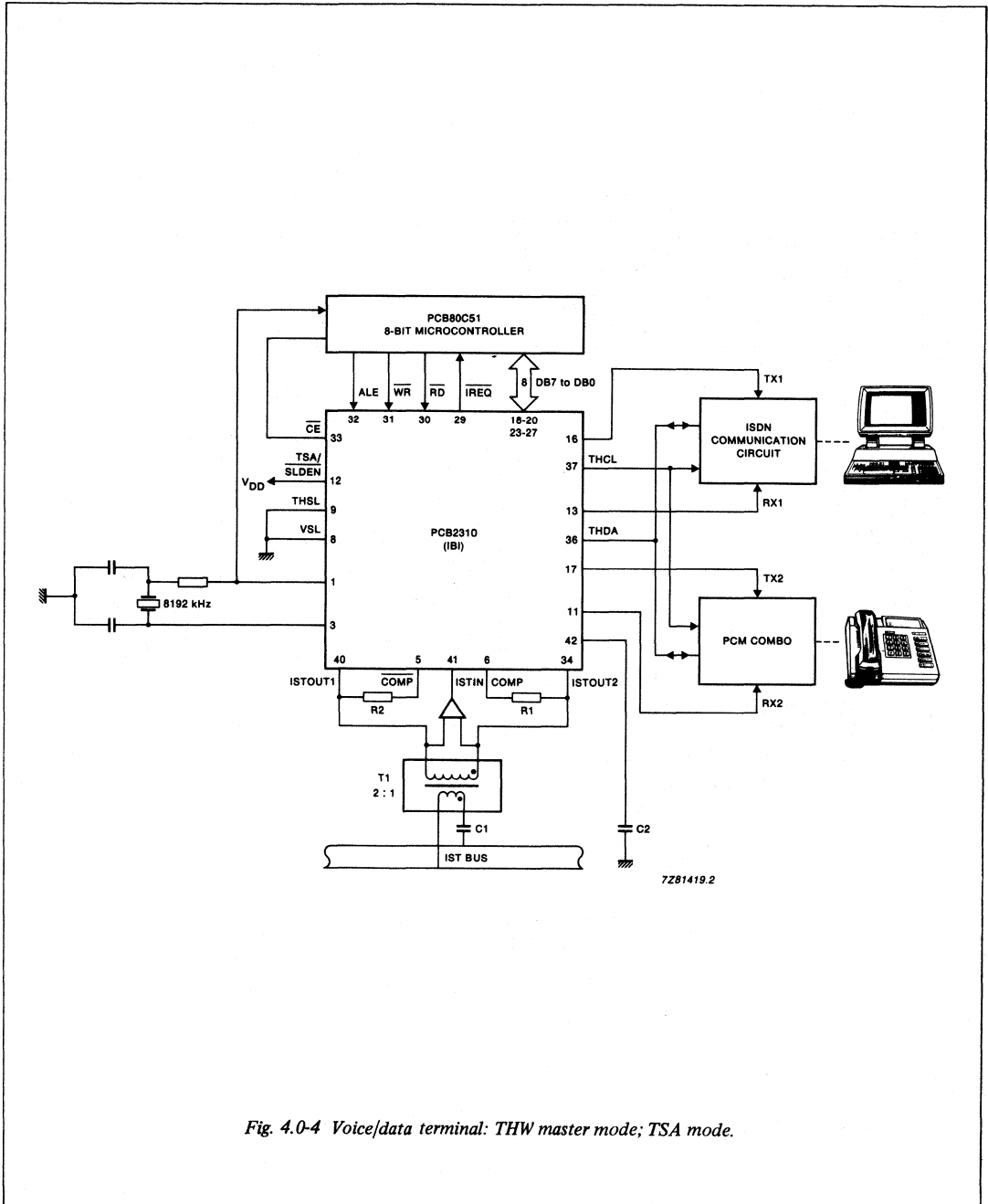
Fig. 4.0-4 Voice/data terminal: THW master mode; TSA mode.

DEVELOPMENT DATA
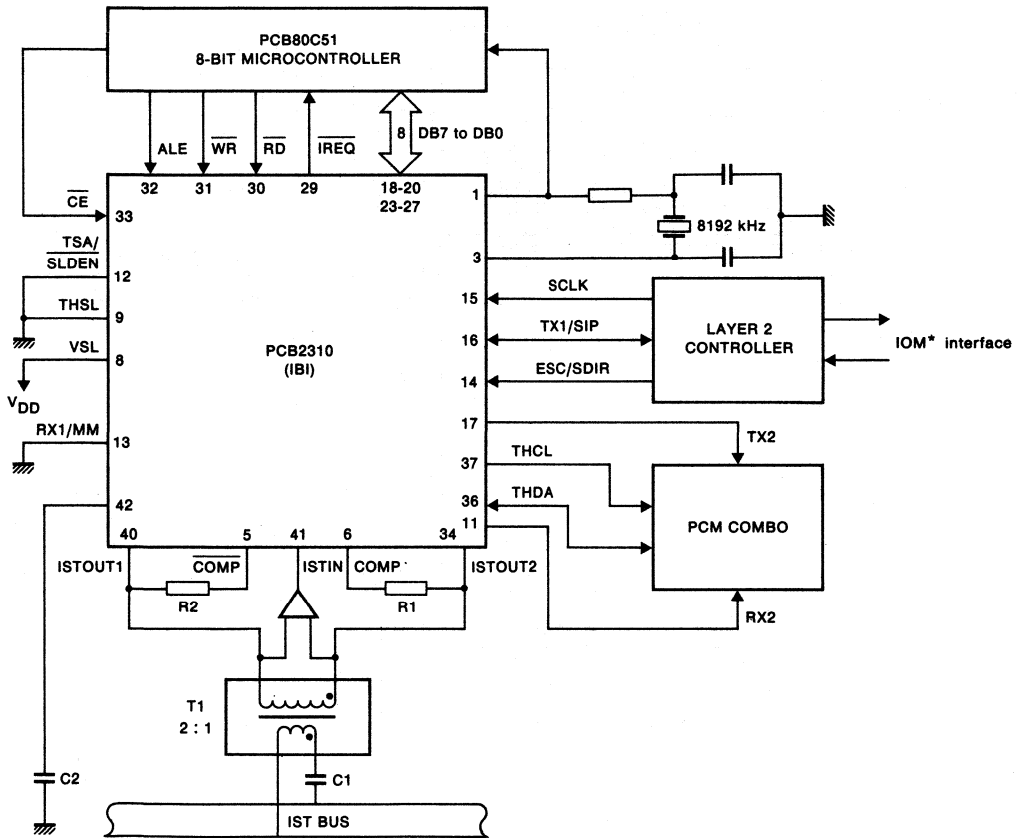
* IOM = ISDN-oriented module.

Fig. 4.0-5 ISDN gateway: combined SLD and TSA mode; THW master mode; SLD slave mode.

EXTRA RINGER

TARIFF METER DISPLAY

TERMINAL ADAPTOR (V24/RS232)

OPTO COUPLER

8.8.8.8.8

PCB80C51 8-BIT MICROCONTROLLER

ALE $\overline{WR}$ $\overline{RD}$ $\overline{IREQ}$

8   DB7 to DB0

$\overline{CE}$

32   31   30   29   18-20 23-27

33

$\frac{TSA/}{SLDEN}$

12

THSL

9

PCB2310 (IBI)

1

3

8192 kHz

RX1/MM

13

V_{DD}

42

40   5   41   6   34

ISTOUT1 $\overline{COMP}$ ISTIN   COMP   ISTOUT2

R2   R1

T1 2 : 1

C1   C2

IST BUS
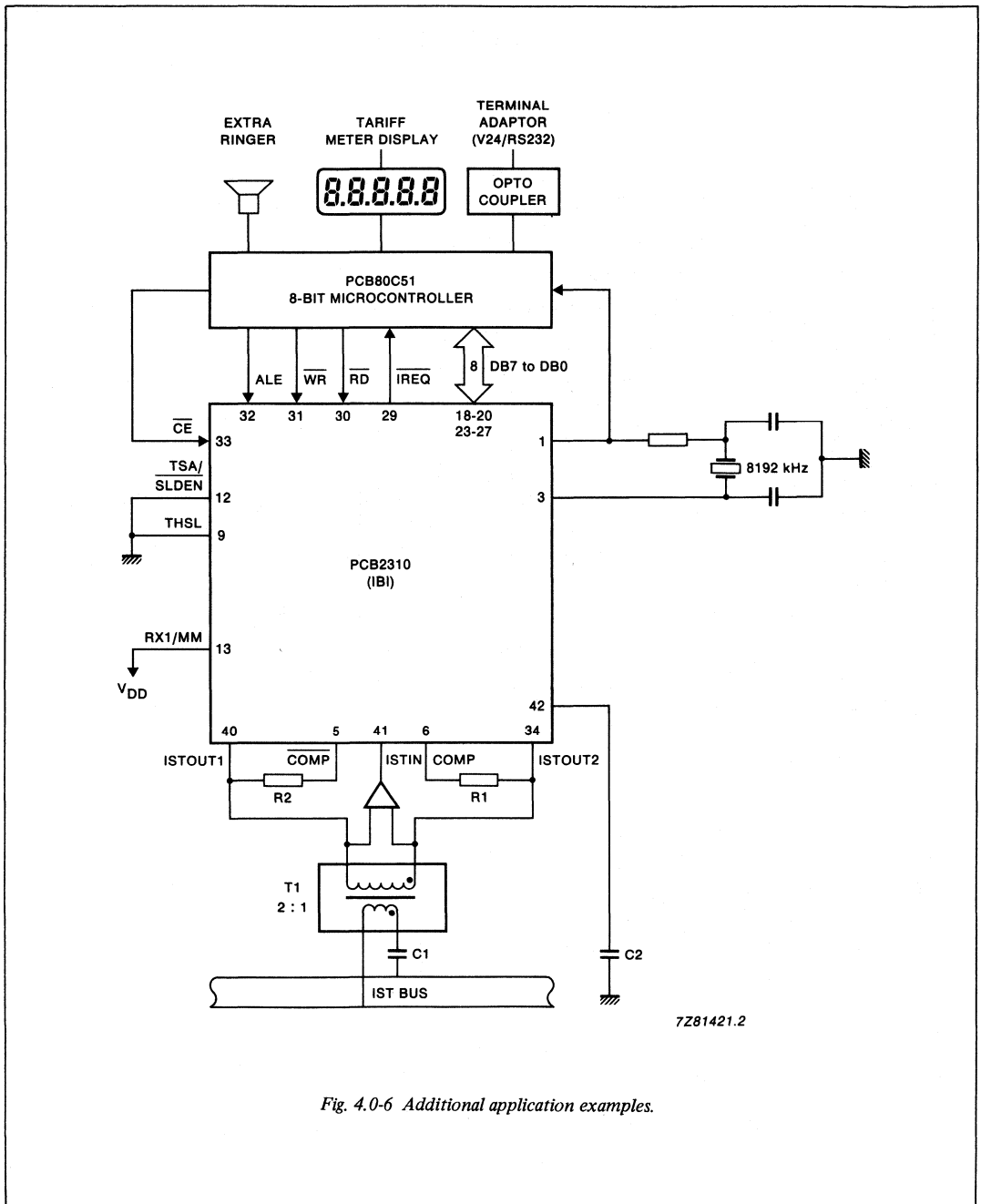
7Z81421.2

Fig. 4.0-6 Additional application examples.

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

PCB2320

DATA RATE ADAPTER

GENERAL DESCRIPTION

The PCB2320 is a CMOS integrated circuit for ISDN applications which has been developed to adapt synchronous and asynchronous user data rates on the CCITT-R interface to a 64 kbit/s Terminal Highway channel (THW).

Features

- Synchronous data rate adaption to 64 kbit/s according to both CCITT X.30 and V.110 specification
- Synchronous data rates supported from 600 to 64000 bits/s
- Asynchronous data rates supported using multisampling method up to 19200 bit/s with additional transition coding based on CCITT recommendation R.111. These rates are of use for 50, 75, 110, 134.5, 150, 200, 3600, 7200, 12000, 14400 and 19200 bits/s
- Automatic speed recognition in receiver with the aid of a microcontroller (for synchronous speeds up to 19200 bits/s)
- 2 Mbit highway interface (long synchronization)
- Serial interface for the DTE
- Microcontroller interface with multiplexed address/data bus
- Interchange circuits mapped into X and S bits
- Forcing and looping of interchange circuits
- Setting of test loops
- DRA monitoring possibilities for in or out of synchronization indication, activity check and readout of the logic states in the interchange circuits
- Single 5 V power supply
- TTL compatible input levels

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117)

Fig.1 Block diagram.

7Z24933

Fig.2 Pinning diagram.

PIN	SYMBOL	DESCRIPTION
1	SCAN	Scantest-mode select. For normal use of the DRA, SCAN should be connected to ground.
2	Q106	Q106 performs as a circuit 106, a CCITT V-series defined interchange circuit. The μC is able to control this circuit (see section 2.4).
3	SCOUT	Scanline output. This output is only used in the scantest mode. For normal use this pin should not be connected.
4	TEST	Test-mode setting. For normal use TEST should be always connected to ground.
5	C20	Clock input (2.048 MHz). C20 is the clock input for the device.
6	HWI	Highway input. Input for the 2 Mbit/s highway time slot (8-bits) timed by C20 (pin 5) and controlled by FS (pin 9).
7	B	Byte timing output (X series). Signal B is a CCITT-X series defined control signal. This circuit provides the byte timing signal for the DTE. The output at pin 7 indicates the last bit of a data byte, it is HIGH during one period of S114/115 (pin 8) and LOW during the byte period. Output B can be controlled by the microcontroller.
8	S114/115	Signal element timing output. S114/115 (circuit 114/115 for V, S for X series) provides signal element timing. In synchronous mode S114/115 generates the data clock for circuit T103 and R104. In asynchronous mode S114/115 generates 48 kHz which is half of the sampling clock frequency of the asynchronous coder. S114/115 can be controlled by the microcontroller.

PIN	SYMBOL	DESCRIPTION
9	FS	Frame select input. Highway frame alignment signal. Every 125 μs FS aligns the 8 highway bits for the DRA on the highway input (pin 6) and highway output (pin 13).
10	CA	Second control input. CA is a signalling channel to the remote subscribers circuit IA. It is sampled every 40 bit frame and transmitted in the X-bit. Output IA can be read by the microcontroller or coupled to Q106. CA can be controlled by the microcontroller.
11	T103	Transmit input. T103 has to be connected to the transmit output (T for X, circuit 103 for V series) of the DTE equipment. For synchronous speeds T103 will be sampled by the DRA on every leading edge of S114/115. T103 can be controlled by the microcontroller.
12	C105	C105 is a signalling channel which corresponds to I109 of the remote subscriber. For the V series, C105 performs as circuit 105 and for the X series as circuit C. C105 is sampled on the trailing edge of the byte-time output pulse. C105 is sampled three times per 40-bit frame and six times per 80-bit multiframe and then placed in the S-bits. C105 can be controlled by the microcontroller.
13	HWO	Highway output. This is the output for the 2 Mbit/s time slot which are produced by the DRA during control of the frame select input. The HWO will be 3-state when FS is LOW. The HWO can be controlled by the microcontroller.
14	GND	System ground.
15	WRCEN	Write chip enable (active LOW). The microcontroller writes data to the DRA when WRCEN is LOW.
16	RDCEN	Read chip enable (active LOW). Data is transferred to the bus by the DRA after the negative edge of RDCEN.
17	DB7	
18	DB6	
19	DB5	
20	DB4	
21	DB3	Data/address bus
22	DB2	
23	DB1	
24	DB0	
25	ALE	Address latch enable input. When ALE is HIGH the data/address bus contains an address.
26	I109	Data channel received line signal detector/indication. Output which indicates the state of the remote subscribers C105 circuit. I109 is inverted on the trailing edge of S114/115. I109 can be made byte-timing synchronous by the microcontroller.
27	R104	R104 provides circuit 104 for the V series and R for the X series of interfaces. Circuit R104 will be shifted out on every trailing edge of S114/115. R104 can be made byte-timing synchronous by the microcontroller.
28	V_{DD}	Power supply + 5 V.

FUNCTIONAL DESCRIPTION

The DRA adapts synchronous user data rates on the 'R' interface in accordance with the CCITT
X.30/V.110 and ECMA 102 specification (September 1984) to a 64-kbit/s THW channel (ISDN
B-channel) and vice-versa. Asynchronous data on the 'R' interface, up to 19200-bits/s, is supported
using the multisampling method with additional transition coding based on the CCITT R.111
recommendation.
The translation between user data rates and the 64-kbit/s data rate is performed in the transmitter and
receiver part as illustrated in Fig.1. The block diagram illustrates three interfaces;

The interchange interface — A set of 'V' type interchange circuits, 103 to 106, 109, 114 and 115
or 'X' type data interface interchange circuits, T, R, C, I, S and B can be connected to the DRA
via level converters.

The terminal highway — The THW is a PCM highway with a transmission rate of 2.048 Mbits/s which
consists of 32 x 64 kbits/s channels. The interface consists of two unidirectional data lines (HWI and
HWO), a THW clock line (C20) and a THW alignment signal line (FS). The internal timing for the
DRA is derived from the THW clock and the THW alignment signal from the clock generator and
synchronization circuit respectively), i.e. no crystal or external oscillator is required.

The 8-bit microcontroller — The microcontroller I/O port is PCB80C51 compatible microcontroller
interface. The data and address lines are multiplexed. The I/O port provides the interface for the
control stages of the DRA. The microcontroller is used to load the DRA with information about
speed, test loops, SET or RESET of interchange circuits while information from the DRA about
speed setting of the remote subscriber, state of the interchange circuits and synchronization on the
THW can be read out.

Modes of operation

For synchronous data rates of 600, 1200, 2400, 4800, 9600, 19200 and 38400-bits/s an X.30/V.110
defined multiframe of 80-bits is used (see Table A1) which consists of 2 x 40-bit frames using
subrates of 8, 16 and 32 kbits/s. An incoming data rate is transposed to the next highest data rate
(the intermediate rate) which is expressed by $2^\wedge$ x 8 kbits/s (where $\wedge$ = 0, 1, 2 or 3, see Table 1).

Table 1 First step in data rate adaption

data rate (bit/s)	frame speed (Hz)
600, 1200, 2400, 4800	8000
9600	16000
19200	32000
38400	64000

The data rate conversion is completed after being multiplied to 64 kbits/s. The multiframe consists of
10 bytes which in turn contains 8 x 6 data bits, 8 x 'S' bits (used for a line signalling channel), 7 bits
to indicate the selected speed and 17 bits for frame synchronization. For a data rate of 48000 bits/s
a 32-bit frame is used (see Table A2). The frame consists of 4 bytes which in turn contain 4 x 6
data bits, 3 x 'S' bits, 1 x 'X' bit and 4 frame synchronization bits. For a data rate of 56000 bits/s
a 32-bit frame is used (see Table A3). The frame consists of 4 x 7 data bits and 4-bits for a line
signalling channel. For a data rate of 64000 bits/s no data rate adaption is required. The DRA is
transparent at this date rate (see Table A4).
For asynchronous data between 0 and 19200 bits/s a transparent transmission method is used. The data
is sampled at 96 kHz and placed in a 48 kbit/s bit-stream. A 32-bit frame is used which consists of
4 x 6 bits for coded data, 3 x 'S' bits, 1 x 'X' bit and 4 frame synchronization bits.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

A coding/sampling method is used which is based on the technique of multiple sampling with additional transition coding, as recommended in CCITT R.111 (see Fig.A1). This method does not recognise character length or start/stop bits but samples the incoming data at 96 kHz and codes the transition in two bits. The resultant 48-kbits/s data stream is inserted in the 32-bit frame in accordance with X.30/V.110. In the 48-kbits/s data stream there are always at least 2 bits per 19.2 kbits/s signal element. One 'T' bit (transition) is used to indicate the polarity after a transition and a second bit 'C' (coding) is used to define in which half, A or B, of the 48 kHz clock period the transition has occured.

Because one bit can discriminate two phases, the sampling frequency must be 96 kHz.

In the lower data rates more than two 48-kbit data bits will fall between two signal element transitions. In this situation the resultant 48-kbit data bits 'P' (polarity) will repeat the polarity and are, therefore, equal to the previous transition bit 'T'.

The phase shift varies for the different bit rates from 20% for 19200 bits/s up to 2.5% for 2400 bits/s (lower for slow data).

Interchange interface

The interchange interface connects the DRA, via level converters, to the DATA Terminal Equipment (DTE) (see Fig.3).

The relationship between the signals on the interchange circuits and the signals at the DRA are given in Table 2. The interchange interface consists of the following circuits:

T103	circuit 103 (V series), transmitted data; T (X series), transmit
R104	circuit 104 (V series), received data; R (X series), receive
C105	circuit 105 (V series), request to send; C (X series), control
Q106	circuit 106 (V series), ready for sending
I109	circuit 109 (V series), data channel received line signal detector; I (X series), indication
S114/115	circuit 114 (V series), transmitter signal element timing circuit 115 (V series), receiver signal element timing; S (X series), signal element timing
B	B (X series), byte timing
CA	second control input
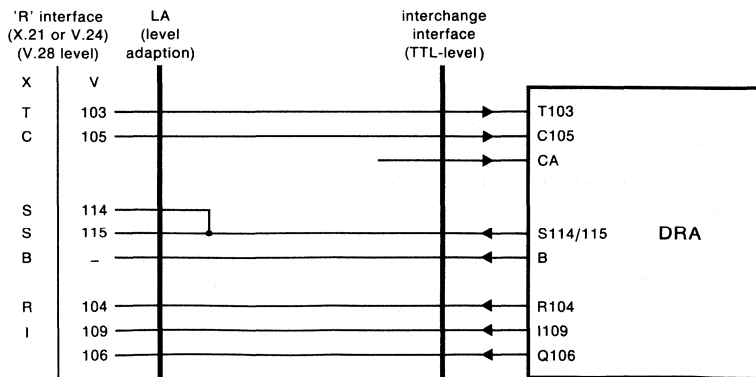
Fig.3 Interchange interface.

Table 2 Relationship between the signals on the interchange circuits and the signals on the DRA.

interchange circuit	state of the int. circuit	pin name of DRA	state on pin of DRA
103 or T	0/1	T103	0/1
104 or R	0/1	R104	0/1
114/115 or S	ON/OFF	S114/115	0/1
B	ON/OFF	B	0/1
105 or C	ON/OFF	C105	0/1
106	ON/OFF	Q106	0/1
109 or I	ON/OFF	I109	0/1
	OFF, 1 : V ⩽ −3 V ON, 0 : V ⩾ 3 V		0: V = 0 V 1: V = 5 V

Note to Table 2

On the highway frame ON = 1 and OFF = 0 in accordance with ECMA 102 (September 1984). This is contrary to ECMA 102 (December 1984 where ON = 0 and OFF = 1).

The frequency of the element timing signal (S114/115 pin 8) is dependent on the data rate setting of the DRA. This can be initiated by bits V1 to V4 in register W1. The relationship between the frequency of S114/115 and the data rate of the DRA is given in Table 5.

The 'B' signal (pin 7) provides the DTE with the byte timing signal. The signal will be HIGH during one period of S114/115 and indicates the last bit of a data byte (LOW during the byte period). The DTE must initiate the first bit of the byte on circuit T103 at the HIGH-to-LOW transition of S114/115 which follows the HIGH-to-LOW transition of signal 'B'. For synchronous speeds T103 (pin 11) is sampled at every leading edge of S114/115 whilst signal changes on R104 (pin 27) occur on every trailing edge (see Fig.4).
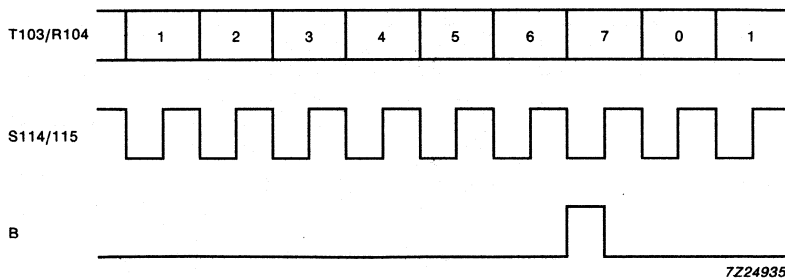
Fig.4 Timing on the interchange interface.

FUNCTIONAL DESCRIPTION (continued)

C105 (pin 12) is sampled on every trailing edge of signal 'B'. It is sampled three times per 40-bit frame and placed in the 'S'-bits of the frame. I109 (pin 26) indicates the state of the remote subscriber circuit C105 and is inverted on the trailing edge of S114/115. I109 can be made byte-timing synchronous under control from the microcontroller.

I109 is delayed to enable an inversion at the first HIGH-to-LOW transition of S114/115 subsequent to the HIGH to LOW transition of circuit 'B' or vice versa. At the same time the 8th data bit is clocked out from R104. I109 is 1-bit earlier as defined in CCITT X.30.

CA is a signalling channel to the remote subscribers circuit IA. The signal is sampled every 40-bit frame and transmitted in the X-bit. Output IA can be read via the microcontroller or coupled to Q106. Signal changes in Q106 occur as soon as the new X-bit is received which is on the falling edge of S114/115.

The sampling moments of the interchange circuits are illustrated in Appendix B.

Terminal highway interface

The terminal highway (THW) is a 2 Mbits/s four-wire fully duplex PCM highway for 64 kbits/s circuit switched channels.

The THW consists of:

HWI	terminal highway input
HWO	terminal highway output
C20	terminal highway 2048 kHz clock input
FS	terminal highway slot assignment input

The THW incorporates 32 channels. One channel, on the HWO, is used to transmit data from the local subscriber to the remote subscriber DTE and one time slot on the HWI to transmit data in the opposite direction. The remaining slots are 'free'. Both the HWI and the HWO are clocked by C20. The slot in which data is transmitted to the THW is aligned by the FS signal. When FS (pin 9) is HIGH the DRA clocks 8 data bits to the HWO and, during this period, data from the HWI is clocked to the DRA. The highway channel assignment is illustrated in Fig.5.

7Z24936
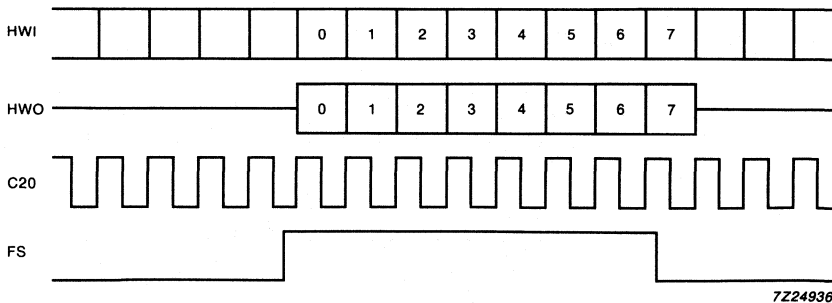
Fig.5 Highway channel assignment.

DEVELOPMENT DATA

8-bit microcontroller interface

The DRA is controlled by the 8-bit microcontroller bus which is compatible with the PCB80C51 microcontroller bus. The microcontroller interface consists of:

8 data/address multiplexed I/O lines (pins 17 to 24)
A read chip enable input (RDCEN pin 16)
A write chip enable (WRCEN pin 15)
An address latch enable (ALE pin 25)

When ALE is HIGH data at the I/O port is latched to the address latch. One of the five write or three read registers can be selected (see Table 3). When RDCEN is LOW the DRA writes data from the selected read register to the I/O port.
When WRCEN is LOW data from the I/O port is written to the selected write register.

Table 3 Register addresses

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	address	WT reg	RD
X	X	X	X	X	0	0	0	0	W0	R0
X	X	X	X	X	0	0	1	1	W1	R1
X	X	X	X	X	0	1	0	2	W2	R2
X	X	X	X	X	0	1	1	3	W3	—
X	X	X	X	X	1	0	0	4	W4	—

The WRITE registers perform the following functions;

- data rate setting
- forcing and looping of the interchange circuits
- setting of test loops

The READ registers can be used to monitor the DRA and have the following functions:

- input/output synchronization indication of the DRA
- activity check on the THW and the interchange circuit T103
- readout the logic state of the interchange circuits
- readout of the data rate setting of the remote DRA

Table 4 Bit assignment registers W0 to W4

WRITE reg	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W0	—	E7	E6	E5	E4	E3	E2	E1
W1	L4	L3	L2	L1	V4	V3	V2	V1
W2	I109	I109	C105	C105	R104	R104	T103	T103
	ON	OFF	ON	OFF	1	0	0	1
W3	DE7	IC	CAI	CI	FS2R	—	CA ON	CA OFF
W4	NC	DR	H1	ND	106 ON	B OFF	106 OFF	S OFF

FUNCTIONAL DESCRIPTION (continued)

Register W0

In every 10 bytes multiframe (for data rates not exceeding 38400 bits/s) bits E1 to E7 are available to transmit information about the data rate to the remote subscriber. The information is described in the X.30/V.110 manuals.
For data rates from 600 to 1200 bits/s E7 is only inserted in the frame when DE7 is at logic 1.
If DE7 is at logic 0 a synchronization pattern will be inserted at E7 in accordance with X.30/V.110.
For data rates from 48000 to 68000 bits/s and the asynchronous mode no E-bits are transmitted.

Register W1

The 'V' bits (V1 to V4) are used to initiate the clock sections of the DRA. The relationship between the data rate and the setting of the 'V' bits is given in Table 5. With each 'L' bit (L1 to L4) a test loop can be created. If L1 is set to logic 1 then T103 (pin 11) is connected to R104 (pin 27). If L2 is set to logic 1 then data received from the remote subscriber is retransmitted back to the remote subscriber. If L3 is set to logic 1 the HWO (pin 13) is connected to HWI (pin 6) and when L4 is set to logic 1 HWI is connected to HWO. The four test loops 1 to 4 are illustrated in Figs 6 and 7.

Table 5 Data rate setting of the DRA

data rate (bits/s)	V4	V3	V2	V1	S114/115 (Hz)
600	1	1	0	0	600
1200	0	0	0	0	1200
2400	1	1	0	1	2400
4800	1	1	1	0	4800
9600	1	1	1	1	9600
19200	0	0	0	1	19200
38400	0	0	1	0	38400
48000	0	0	1	1	48000
56000	0	1	0	0	56000
64000	0	1	0	1	64000
async	0	1	1	1	48000

Register W2

With T103 0 and T103 1 it is possible to clamp the input of T103 to logic 0 or logic 1 or have the data input to the DRA at pin 11. The logic settings for T103 are given in Table 6.
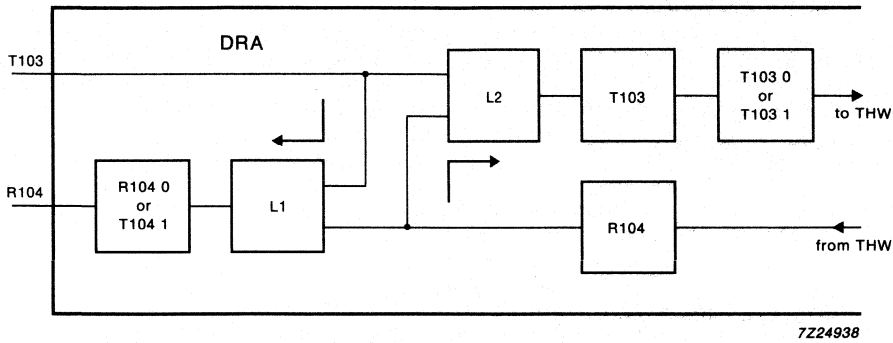
Fig.6 Test loop 1 and 2.
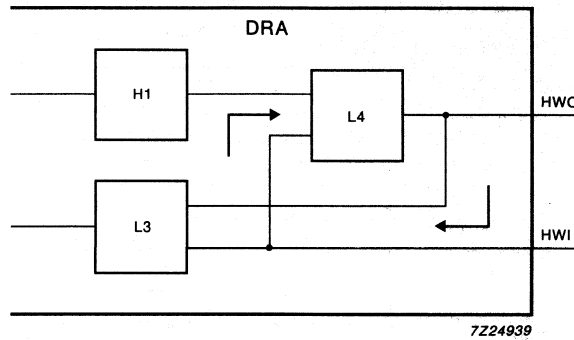
Fig.7 Test loop 3 and 4.

Table 6 Settings for T103 0 and T103 1

T103 1	T103 0	T103
0	0	DRA accepts data at input T103
0	1	input T103 clamped to logic 0
1	0	input T103 clamped to logic 1
1	1	input T103 clamped to logic 1

With R104 0 and R104 1, it is possible to clamp output R104 (pin 27) to logic 0 or logic 1, or, to indicate the received data bits on output R104. The settings for R104 are given in Table 7 (see also Fig.6).

Table 7 Settings for R104 0 and R104 1

R104 0	R104 1	R104
0	0	output R104 indicates the received data bits
0	1	output R104 clamped to logic 1
1	0	output R104 clamped to logic 0
1	1	output R104 clamped to logic 0

FUNCTIONAL DESCRIPTION (continued)

With C105 ON and C105 OFF it is possible to clamp the input C105 (pin 12) to logic 0 or logic 1, or, for the DRA to accept an input on C105. The settings for C105 are given in Table 8 (see also Fig.8).

Table 8 Settings for C105 ON and C105 OFF

C105 ON	C105 OFF	C105
0	0	DRA accepts data at input C105
0	1	input C105 clamped to logic 0
1	0	input C105 clamped to logic 1
1	1	input C105 clamped to logic 1

With I109 ON and I109 OFF it is possible to clamp output I109 (pin 26) to logic 0 or logic 1, or, to indicate the received data bits on output I109. The settings for I109 are given in Table 9 (see also Fig.8).

Table 9 Settings for I109 ON and I109 OFF

I109 OFF	I109 ON	I109
0	0	output I109 indicates the received 'S' bits
0	1	output I109 clamped to logic 0
1	0	output I109 clamped to logic 1
1	1	output I109 clamped to logic 1

Register W3

With CA ON and CA OFF it is possible to clamp the input CA (pin 10) to logic 0 or logic 1, or, for the DRA to accept an input on C105. The settings for CA ON and CA OFF are given in Table 10 (see also Fig.8).

Table 10 Settings for CA ON and CA OFF

CA OFF	CA ON	CA
0	0	DRA accepts data at input CA
0	1	input CA clamped to logic 0
1	0	input CA clamped to logic 1
1	1	input CA clamped to logic 1

The FS2R bit controls the 4-byte synchronization system for data rates greater than 38400 bits/s and asynchronous. When set to logic 1 the incoming highway data is assumed to be byte synchronous and the DRA will only search on the first bit position of every HW octet for synchronization. When set to logic 1 the DRA will search for synchronization on every bit position.

Because this may cause wrong synchronization on the 'S' and 'X' (the 8th bit) instead of the first bit the CCITT recommends that this mode be used only for international purposes and, in this case, make the 'X' bit a continuous logic 1 (by making CA logic 0).

If CI is set to logic 0 then data at input C105 is placed in the 'S' bits to be transferred. If CI is set to logic 1 then the 'S' bits received on the THW are placed in the 'S' bits to be transferred (see Fig.8).

If CAI is set to logic 0 then data at the CA input is placed in the 'X' bits to be transferred. If CAI is set to logic 1 then the 'S' bits received on the THW are placed in the 'X' bits to be transferred (see Fig.8).

If IC is set to logic 0 then the 'S' bits received on the THW are placed at output I109. If IC is set to logic 1 then output I109 is connected to input C105 (see Fig.8).
If DE7 is set to logic 0, for data rates 600 and 1200 bits/s, a synchronization pattern will be inserted at E7 in the frame (the synchronization pattern for a data rate of 600 bits/s is specified in CCITT X.30). If DE7 is set to logic 1 the synchronization pattern will be disabled and position E7 in the frame will be filled with information from W0. The synchronization pattern is given in Tables 11 and 12.

Table 11 The synchronization pattern at E7 for 1200 bits/s

multiframe 1	00000000	1PPPPPPS 111122	1PPPPPPX 223333	1PPPPPPS 444455	1PPPPPPS 556666
	1EEEEEE1 123456	1PPPPPPS 777788	1PPQQQQX 881111	1QQQQQQS 222233	1QQQQQQS 334444
multiframe 2	00000000	1QQQQQQS 555566	1QQQQQQX 667777	1QQQQRRS 888811	1RRRRRRS 112222
	1EEEEEEO 123456	1RRRRRRS 333344	1RRRRRRX 445555	1RRRRRRS 666677	1RRRRRRS 778888

Table 12 The synchronization pattern at E7 for 600 bits/s

multiframe 1	00000000	1PPPPPPS 111111	1PPPPPPX 112222	1PPPPPPS 222233	1PPPPPPS 333333
	1EEEEEE1 123456	1PPPPPPS 444444	1PPPPPPX 445555	1PPPPPPS 555566	1PPPPPPS 666666
multiframe 2	00000000	1PPPPPPS 777777	1PPPPPPX 778888	1PPPPQQS 888811	1QQQQQQS 111111
	1EEEEEE1 123456	1QQQQQQS 222222	1QQQQQQX 223333	1QQQQQQS 333344	1QQQQQQS 444444
multiframe 3	00000000	1QQQQQQS 555555	1QQQQQQX 556666	1QQQQQQS 666677	1QQQQQQS 777777
	1EEEEEE1 123456	1QQQQQQS 888888	1QQRRRRX 881111	1RRRRRRS 111122	1RRRRRRS 222222
multiframe 4	00000000	1RRRRRRS 333333	1RRRRRRX 334444	1RRRRRRS 444455	1RRRRRRS 555555
	1EEEEEEO 123456	1RRRRRRS 666666	1RRRRRRX 667777	1RRRRRRS 777788	1RRRRRRS 888888

After two multiframes the E7 bit changes from logic 1 to logic 0. This indicates that three complete data bytes have been transmitted.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION   (continued)

Register W4

If S OFF is set to logic 1 S114/115 will be forced to logic 1.

If B OFF is set to logic 1 B will be forced to logic 1.

With 106 ON and 106 OFF it is possible to clamp output Q106 (pin 2) to logic 1 or logic 0, or, for Q106 to indicate the received X-bits. The settings for 106 ON and 106 OFF are given in Table 13.

Table 13 Settings for 106 ON and 106 OFF

106 OFF	106 ON	Q106
0	0	output Q106 indicates the received X bits
0	1	output Q106 clamped to logic 0
1	0	output Q106 clamped to logic 1
1	1	output Q106 clamped to logic 1

When ND is set to logic 0 R104 and I109 become byte-timing synchronous. This is realized by delaying the incoming data from the remote subscriber. For 'V' series interfaces no byte-timing is requested. When ND is set to logic 1 R104 and I109 are not byte-timing synchronous and no extra delay is inserted.

When H1 is set to logic 1 the HWO will be clamped internally to logic 1 (see Fig.7).

In the receiver section of the DRA a synchronization system searches for the E7 synchronization bits for data at 600 and 1200 bits/s. When DR is set to logic 1 the synchronization system will be switched OFF consequently R104 and I109 will not be byte-timing synchronous.

If ND is set to logic 0 the I109 signal change can be timed in two modes. When NC (no CCITT) is set to logic 0 the I109 signal will be inverted at the first logic 1 to logic 0 transition of S114/115 after the logic 1 to logic 0 transition of 'B'. When NC is set to logic 1 I109 will be inverted at the logic 1 to logic 0 transition of S114/115 when 'B' is set to logic 1. At the same time the 8th data bit will be clocked out on R104 (I109 is one bit earlier as defined in CCITT X.30).
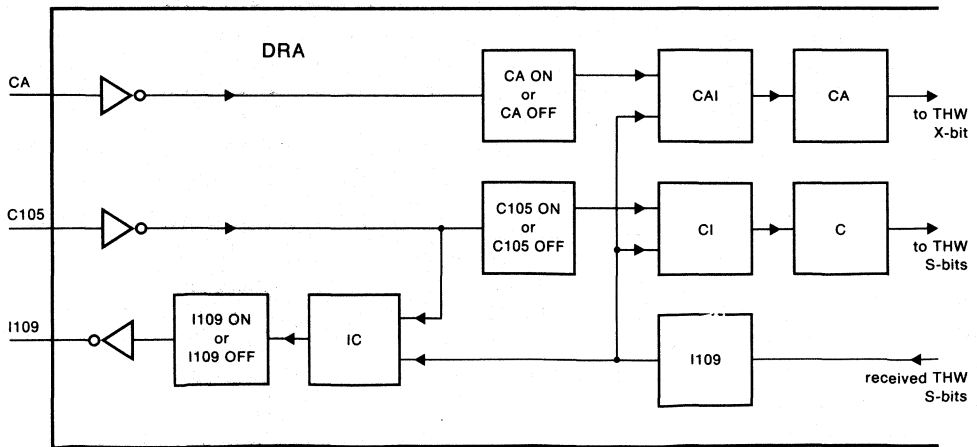
7Z24940

Fig.8 Interchange loops.

Registers R0 to R2

Table 14 Bit assignment registers R0 to R2

reg	7	6	5	4	3	2	1	0
R0	—	E7	E6	E5	E4	E3	E2	E1
R1	—	—	T103	R104	IA	I109	CA	C
R2	—	—	—	—	ACTT	ACTR	OOS	AL

Register R0

In every 10-byte multiframe (for data rates not exceeding 38400 bits/s) bits E1 to E7 are available to transmit information concerning the data rate.

The information that is inserted by the remote subscriber is received in these bits. For data rates of 600 and 1200 bits/s, bit 7 is only inserted in the frame when DE7 is set to logic 1.

If DE7 is set to logic 0 a synchronization pattern will be inserted at E7 in accordance with CCITT X.30/V.110.

For data rates from 48000 to 64000 bits/s and the asynchronous mode, no 'E' bits are received.

Register R1

Bit 'C' indicates the conditions of C105. If 'C' is set to logic 0 then C105 is OFF. The transmission S-bits are set to logic 0 (see Fig.8).

Bit CA indicates the condition of signal CA. If CA is set to logic 0 the signal will be OFF. The transmitted X-bits are set to logic 0 (see Fig.8).

Bit I109 indicates the condition of signal I109. If the received S-bits are set to logic 0 the bit I109 will be set to logic 0 (see Fig.8).

Bit IA is set to logic 0 if the received X-bits are at logic 0 (see Fig.8).

Bit R104 indicates the condition of signal R104. If the received data bits are at logic 0, R104 will be set to logic 0.

Bit T103 indicates the condition of signal T103. If bit T103 is at logic 0 signal T103 will be at logic 0. The transmitted data bits are set to logic 0.

Register R2

Bit AL indicates the out of synchronization (OOS) of the receiver between two successive readouts. Immediately after the readout the bit is reset. If the OOS bit is set to logic 0 then the DRA is in synchronization and at logic 1 is out of synchronization. The synchronization check is performed by the receiver section and is required to synchronize the internal clock generator for frame encoding (i.e. checks that the frame bits are correctly positioned in the frame). If the frame bits are not correctly positioned the following should be verified;

● The clock unit is preset to the correct position
● Frame bits have not been distorted. The DRA sends an OOS after three consecutive incorrect multiframes (with one or more errors per multiframe) then begins to search for the correct timing
  ● after receiving eight zero frame bits the clock unit is preset to the correct position
  ● if the following frame bits in that multiframe are received correctly the DRA is assumed to be in synchronization and the OOS bit will be reset
  ● if the frame bits are not all correct the OOS bit will remain at logic 1 and the DRA will search for the next eight zero frame bits

Bit ACTR checks the activity of the remote subscriber by controlling the incoming highway.

Activity — ACTR = logic 1
No activity — ACTR = logic 0

After reading the register the bits are automatically set to zero ready for the next activity check.
Bit ACTT checks the activity of the local DTE transmit circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
DC supply voltage		V_{DD}	-0.5	7.0	V
DC supply current		$\pm I_{DD}$	—	50	mA
DC ground current		$\pm I_{GND}$	—	30	mA
DC input diode current	$V_I < -0.5$ or $V_I > V_{DD} + 0.5$ V	$\pm I_{IK}$	—	20	mA
DC output diode current	$V_O < -0.5$ or $V_O > V_{DD} + 0.5$ V	$\pm I_{OK}$	—	20	mA
Storage temperature range		T_{stg}	-65	$+150$	^{o}C
Operating ambient temperature range		T_{amb}	0	70	^{o}C
Total power dissipation		P_{tot}	—	500	mW

DEVELOPMENT DATA

DC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$; voltages are referenced to ground

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Quiescent supply current	$V_{DD} = 5.5\ V$	I_{DD}	–	–	50	μA
INPUTS						
Input voltage HIGH						
CMOS input pin 4 (test)	$V_{DD} = 4.5$ to $5.5\ V$	V_{IH}	$0.7 \times V_{DD}$	–	–	V
TTL inputs and I/Os	$V_{DD} = 4.5$ to $5.5\ V$	V_{IH}	2.0	–	–	V
Input voltage LOW						
CMOS input pin 4 (test)	$V_{DD} = 4.5$ to $5.5\ V$	V_{IL}	–	–	$0.3 \times V_{DD}$	V
TTL inputs and I/Os	$V_{DD} = 4.5$ to $5.5\ V$	V_{IL}	–	–	0.8	V
Input leakage current	$V_I = V_{DD}$ or GND	$\pm I_I$	–	–	0.1	μA
OUTPUTS						
Output 1 (pins 2,3,7,8,26 and 27)						
Output voltage LOW	$V_{DD} = 5\ V$ $I_{OL} = 1.5\ mA$	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD} = 5\ V$ $-I_{OH} = 2\ mA$	V_{OH}	2.4	–	–	V
Output 2 (pins 13 and 18 to 24)						
Output voltage LOW	$V_{DD} = 5\ V$ $I_{OL} = 4.5\ mA$	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD} = 5\ V$ $-I_{OH} = 3\ mA$	V_{OH}	4.3	–	–	V
3-state OFF current	$V_O = V_{DD}$ or GND $I_O = 0$	$\pm I_{OZ}$	–	–	0.5	μA

AC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance		C_I	–	–	10	pF
Input/output capacitance		$C_{I/O}$	–	–	20	pF

TIMING CHARACTERISTICS

$T_{amb} = 25\ ^{\circ}C$; $V_{DD} = 5$ V; GND = 0 V

parameter	conditions	symbol	min.	typ.	max.	unit
TERMINAL HIGHWAY						
C20						
Clock period		tw_C	—	488	—	ns
FS						
Delay time with reference to C20		td_{CLFH}	50	—	150	ns
		td_{CHFL}	50	—	430	ns
HWI						
Data set-up time		ts_I	100	—	—	ns
HWO						
Rise time	CL = 30 pF	tt_{LH}	—	—	30	ns
Fall time	CL = 30 pF	tt_{HL}	—	—	30	ns
Data set-up time		ts_O	—	—	50	ns
INTERCHANGE INTERFACE						
S114/115						
Rise time	CL = 30 pF	tt_{LH}	—	—	100	ns
Fall time	CL = 30 pF	tt_{HL}	—	—	100	ns
T103						
Data set-up time		ts_T	100	—	—	ns
Data hold time		th_T	0	—	—	ns
R104						
Rise time	CL = 30 pF	tt_{LH}	—	—	100	ns
Fall time	CL = 30 pF	tt_{HL}	—	—	100	ns
Data set-up time		ts_{SR}	—	—	100	ns
C105						
Data set-up time		ts_{BC}	100	—	—	ns
Data hold time		th_{BC}	0	—	—	ns
Q106						
Rise time	CL = 30 pF	tt_{LH}	—	—	100	ns
Fall time	CL = 30 pF	tt_{HL}	—	—	100	ns
Data set-up time		ts_{SQ}	—	—	100	ns

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
I109						
Rise time	CL = 30 pF	tt_{LH}	—	—	100	ns
Fall time	CL = 30 pF	tt_{HL}	—	—	100	ns
Data set-up time		ts_{SI}	—	—	100	ns
CA						
Data set-up time		ts_C	100	—	—	ns
Data hold time		th_C	0	—	—	ns
B						
Rise time	CL = 30 pF	tt_{LH}	—	—	100	ns
Fall time	CL = 30 pF	tt_{HL}	—	—	100	ns
MICROCONTROLLER BUS						
ALE pulse width		tw_A	100	—	—	ns
Data bus READ cycle						
Address set-up time		ts_A	25	—	—	ns
Address hold time		th_A	10	—	—	ns
RDCEN pulse width		tw_R	500	—	—	ns
READ access time	CL = 200 pF	ta_R	—	—	200	ns
Data hold time		th_D	10	—	—	ns
Time from RDCEN HIGH to ALE LOW		td_{RA}	1	—	—	μs
Data bus WRITE cycle						
Address set-up time		ts_A	25	—	—	ns
Address hold time		th_A	10	—	—	ns
WRCEN pulse width		tw_W	100	—	—	ns
Data set-up time		ts_D	10	—	—	ns
Data hold time		th_D	10	—	—	ns
Time from WRCEN HIGH to ALE LOW		td_{WA}	10	—	—	ns

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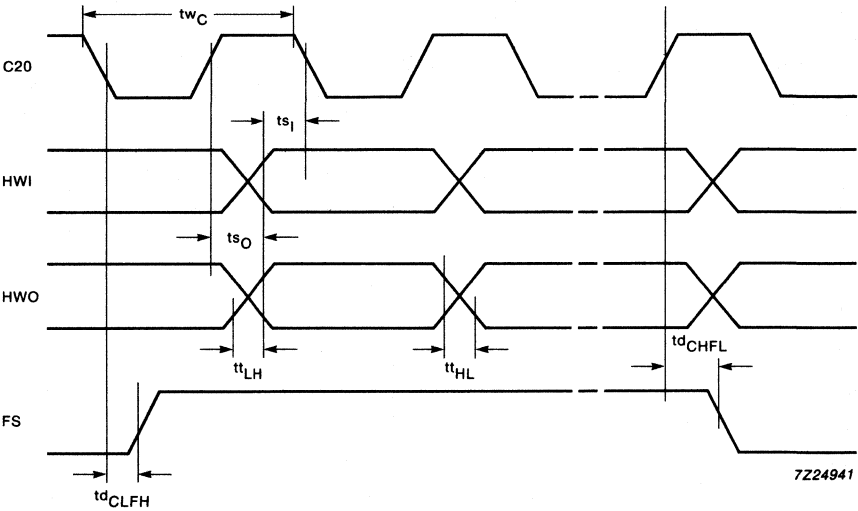
Fig.9 Terminal highway timing diagram.

DEVELOPMENT DATA
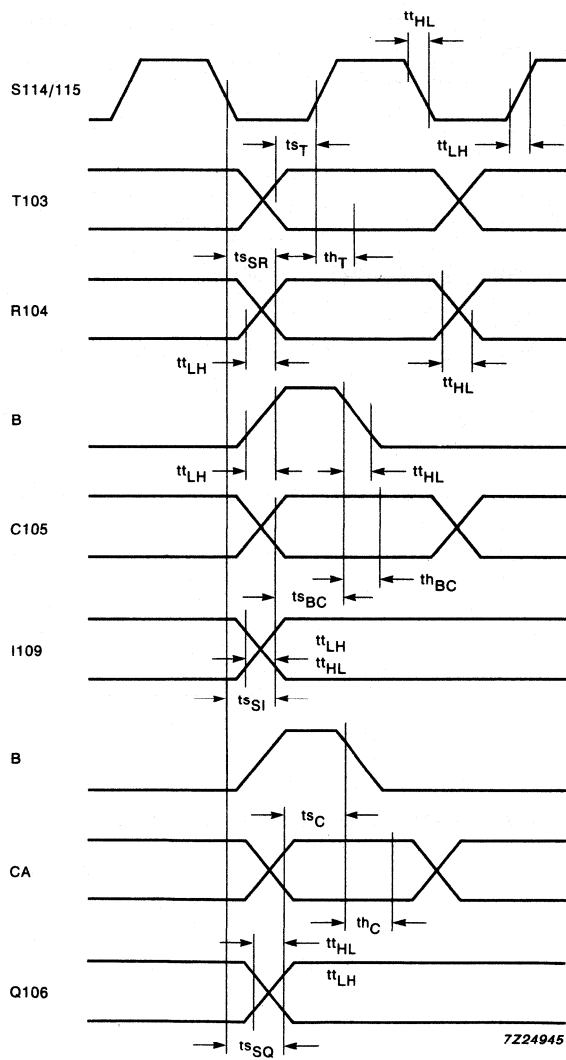
Fig.10 Interchange interface timing diagram.
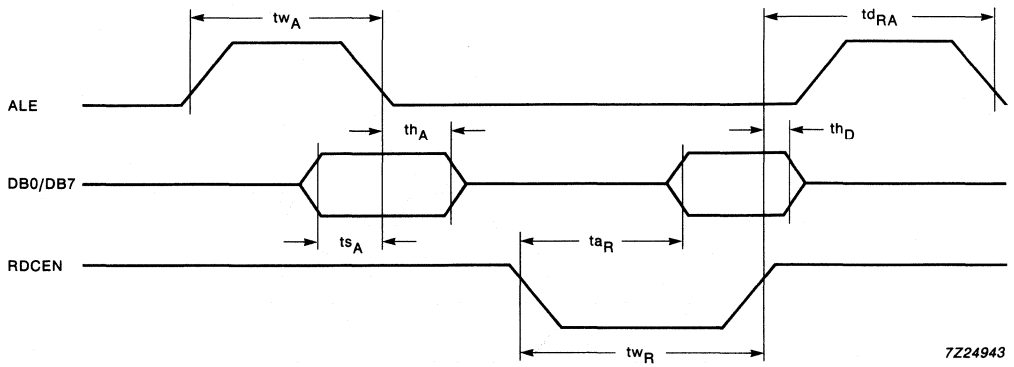
Fig.11 Data bus READ cycle timing diagram.
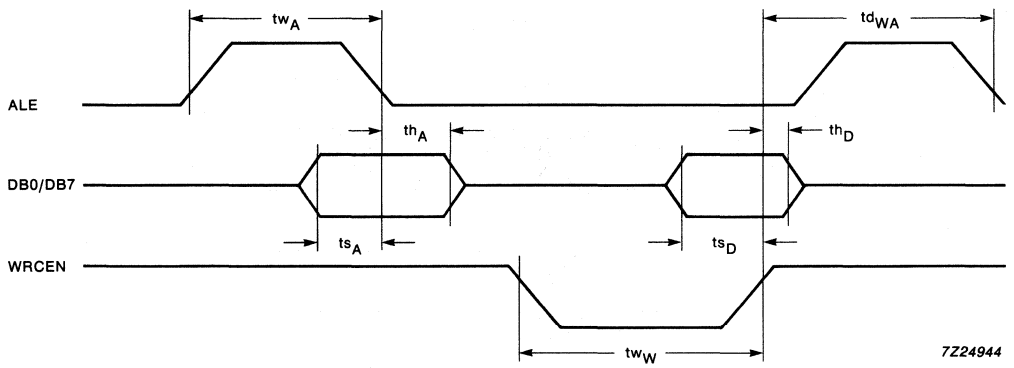
Fig.12 Data bus WRITE cycle timing diagram.

APPENDIX A

INTERMEDIATE FRAME FORMATS

Table A1 Frame format for the intermediate datastream for synchronous user data rates when no bit repetition is used (4800, 9600 and 19200 bits/s).

OCTET	bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1/P1	D2/P2	D3/P3	D4/P4	D5/P5	D6/P6	S1/SQ
2	1	D7/P7	D8/P8	D9/Q1	D10/Q2	D11/Q3	D12/Q4	X
3	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
4	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D25/P1	D26/P2	D27/P3	D28/P4	D29/P5	D30/P6	S6/SQ
7	1	D31/P7	D32/P8	D33/Q1	D34/Q2	D35/Q3	D36/Q4	X
8	1	D37/Q5	D38/Q6	D39/Q7	D40/Q8	D41/R1	D42/R2	S8/SR
9	1	D43/R3	D44/R4	D45/R5	D46/R6	D47/R7	D48/R8	S9/SP

Frame format on the terminal highway for the synchronous user data rate of 38400 bits/s (V.110/X.30).

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 106 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

Table A2 Frame format of the intermediate data stream (8 kbits/s) with a synchronous user data rate of 2400 bits/s (V.110/X.30).

OCTET	bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1/P1	D1/P1	D2/P2	D2/P2	D3/P3	D3/P3	S1/SP
2	1	D4/P4	D4/P4	D5/P5	D5/P5	D6/P6	D6/P6	X
3	1	D7/P7	D7/P7	D8/P8	D8/P8	D9/Q1	D9/Q1	S3/SQ
4	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S4/SQ
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S6/SR
7	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D18/R2	D18/R2	X
8	1	D19/R3	D19/R3	D20/R4	D20/R4	D21/R5	D21/R5	S8/SR
9	1	D22/R6	D22/R6	D23/R7	D23/R7	D24/R8	D24/R8	S9/SP

DEVELOPMENT DATA

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

Table A3 Frame format of the intermediate datastream (8 kbits/s) for a synchronous user data rate of 1200 bits/s (V.110).

OCTET	bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1	D1	D1	D1	D2	D2	S1
2	1	D2	D2	D3	D3	D3	D3	X
3	1	D4	D4	D4	D4	D5	D5	S3
4	1	D5	D5	D6	D6	D6	D6	S4
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D7	D7	D7	D7	D8	D8	S6
7	1	D8	D8	D9	D9	D9	D9	X
8	1	D10	D10	D10	D10	D11	D11	S8
9	1	D11	D11	D12	D12	D12	D12	S9

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA	S1, S3, S4, S6, S8, S9 X	109 IA (microcontroller read) 106
	103	D1 to D48	104

Table A4 Frame format of the intermediate datastream (8 kbits/s) for the user data rate of 600 bits/s (V.110/X.30).

OCTET	bit number							
	1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	D1/P1	D1/P1	D1/P1	D1/P1	D1/P1	D1/P1	S1/SP
2	1	D1/P1	D1/P1	D2/P2	D2/P2	D2/P2	D2/P2	X
3	1	D2/P2	D2/P2	D2/P2	D2/P2	D3/P3	D3/P3	D3/SP
4	1	D3/P3	D3/P3	D3/P3	D3/P3	D3/P3	D3/P3	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D4/P4	D4/P4	D4/P4	D4/P4	D4/P4	D4/P4	S6/SP
7	1	D4/P4	D4/P4	D5/P5	D5/P5	D5/P5	D5/P5	X
8	1	D5/P5	D5/P5	D5/P5	D5/P5	D6/P6	D6/P6	S8/SP
9	1	D6/P6	D6/P6	D6/P6	D6/P6	D6/P6	D6/P6	S9/SP
0	0	0	0	0	0	0	0	0
1	1	D7/P7	D7/P7	D7/P7	D7/P7	D7/P7	D7/P7	S1/SP
2	1	D7/P7	D7/P7	D8/P8	D8/P8	D8/P8	D8/P8	X
3	1	D8/P8	D8/P8	D8/P8	D8/P8	D9/Q1	D9/Q1	S3/SP
4	1	D9/Q1	D9/Q1	D9/Q1	D9/Q1	D9/Q1	D9/Q1	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	S6/SQ
7	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D11/Q3	D11/Q3	X
8	1	D11/Q3	D11/Q3	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S8/SQ
9	1	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	S9/SP
0	0	0	0	0	0	0	0	0
1	1	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	S1/SP
2	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D14/Q6	D14/Q6	X
3	1	D14/Q6	D14/Q6	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S3/SP
4	1	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	S6/SQ
7	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D17/R1	D17/R1	X
8	1	D17/R1	D17/R1	D17/R1	D17/R1	D18/R2	D18/R2	S8/SQ
9	1	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	S9/SP
0	0	0	0	0	0	0	0	0
1	1	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	S1/SP
2	1	D19/R3	D19/R3	D20/R4	D20/R4	D20/R4	D20/R4	X
3	1	D20/R4	D20/R4	D20/R4	D20/R4	D21/R5	D21/R5	S3/SP
4	1	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	S4/SP
5	1	E1	E2	E3	E4	E5	E6	E7
6	1	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	S6/SQ
7	1	D22/R6	D22/R6	D23/R7	D23/R7	D23/R7	D23/R7	X
8	1	D23/R7	D23/R7	D23/R7	D23/R7	D24/R8	D24/R8	S8/SQ
9	1	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	S9/SP

DEVELOPMENT DATA

Table 4 (continued)

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4, S6, S8, S9 X D1 to D48	109 IA (microcontroller read) 106 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

Table A5 Frame format on the terminal highway for synchronous user data of 48 kbits/s and asynchronous user data rates up to 19.2 kbits/s (V series only).

OCTET	bit number							
	1	2	3	4	5	6	7	8
1	1	D1/P1	D2/P2	D3/P3	D4/P4	D5/P5	D6/P6	S1/SQ
2	0	D7/P7	D8/P8	D9/Q1	D10/Q2	D11/Q3	D12/Q4	X
3	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
4	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S1, S3, S4 X D1 to D24	109 IA (microcontroller read) 106 104
X series	C CA T	SP, SQ, SR X P1 to R8	I IA (microcontroller read) R

DEVELOPMENT DATA

Table A6 Frame format on the terminal highway for synchronous data rates of 56 kbits/s. When 'S' is set to logic 1 the frame will comply to V.110.

OCTET	bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	S
2	D8	D9	D10	D11	D13	D13	D14	S
3	D15	D16	D17	D18	D19	D20	D21	S
4	D22	D23	D24	D25	D26	D27	D28	S

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105 CA 103	S no transmission D1 to D28	109 IA (microcontroller read) 106 104
X series	C CA T	S no transmission D1 to D28	I IA (microcontroller read) R

Table A7 Frame format on the terminal highway for synchronous data rates of **64 kbits/s**

OCTET	bit number							
	1	2	3	4	5	6	7	8
1	D1	D2	D3	D4	D5	D6	D7	D8
2	D9	D10	D11	D12	D13	D14	D15	D16
3	D17	D18	D19	D20	D21	D22	D23	D24
4	D25	D26	D27	D28	D29	D30	D31	D32

	from interchange circuits of local subscriber	frame bits	to remote subscriber
V series	105	no transmission	109
	CA	no transmission	IA (microcontroller read)
			106
	103	D1 to D32	104
X series	C	no transmission	I
	CA	no transmission	IA (microcontroller read)
	T	D1 to D32	R

DEVELOPMENT DATA

APPENDIX B

SAMPLE MOMENTS OF THE INTERCHANGE CIRCUITS

asynchronous signal

A | B | A | B | A | B | A | B | A | B | A | B | A | B | A | B | A |

96 kHz

48 kHz

T   C   P   T   C   T   C   P

bit identity

1   0   1   0   0   1   0   1
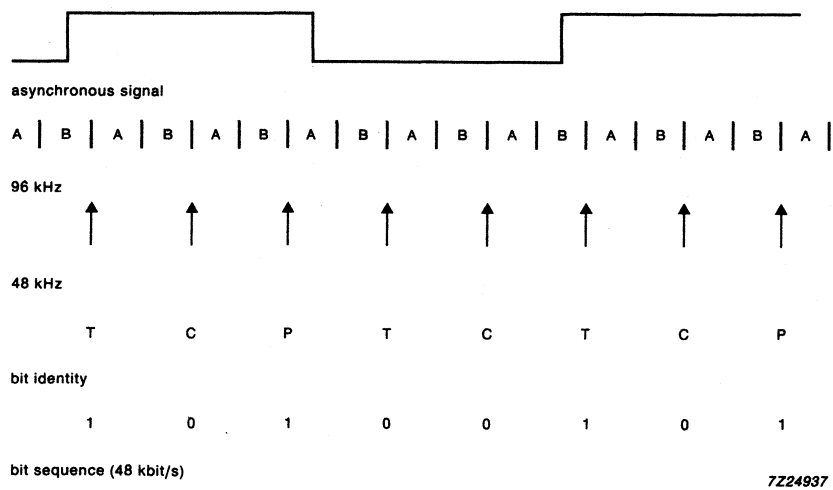
bit sequence (48 kbit/s)   7Z24937

code character for a transition (C)		position of the transition in a group of two sampling pulses
from 1 to 0	from 0 to 1	
T C	T C	
0 0	1 1	in first half (A)
0 1	1 0	in second half (B)

Additional transition coding is based on R.111. However, in R.111, two transition code characters (C1 and C2) are used for each signal transition instead of one (C).

Fig.A1 Additional transition coding.

DEVELOPMENT DATA
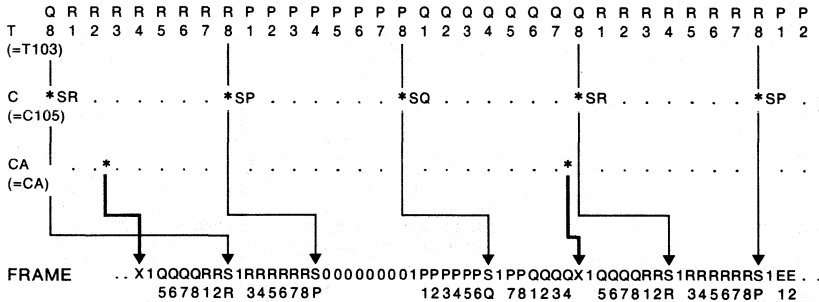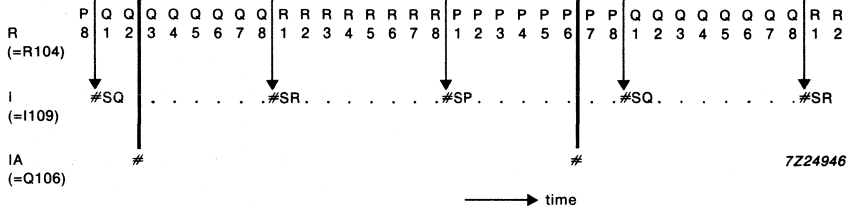
TRANSMITTER:

```
      Q R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R R R R R R R P P
T     8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2
(=T103)

C     *SR . . . . . . *SP . . . . . . *SQ . . . . . . *SR . . . . . . *SP .
(=C105)

CA    . . * . . . . . . . . . . . . . . . . . . . . . * . . . . . . . . . .
(=CA)

FRAME  . . X1QQQQRRS1RRRRRRS000000001PPPPPPS1PPQQQQX1QQQQRRS1RRRRRRS1EE . .
                567812R 345678P        123456Q 781234 567812R 345678P 12

RECEIVER:

      P Q Q Q Q Q Q Q R R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R
R     8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2
(=R104)

I     #SQ . . . . . . #SR . . . . . . .#SP . . . . . . .#SQ . . . . . . .#SR
(=I109)

IA       #                             #                          7Z24946
(=Q106)
```

→ time

Notes

* sample moment of the interchange circuit
# change point of the interchange circuit

When bit repetition is used (600 and 2400 bits/s) the value of the last sample of the interchange circuits is repeated in the 'S' and 'X' data bits until a new sample is made (see Appendix A Table A2 and A4).

Fig.B1 Sample moments and change points of the interchange circuit C, CA, IA and I using a 10-byte frame (REC. X.30).

TRANSMITTER:

```
T
(=T103)
            Q R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R R R R R R P P
            8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2

C           . . . . . . *SP . . . . . . . *SQ . . . . . . *SR . . . . . . *SP
(=C105)

CA
(=CA)                                         *

FRAME       . . . 1 R R R R R R S 1 P P P P P P S 0 P P Q Q Q Q X 1 Q Q Q Q R R S 1 R R R R R R S 1 . . .
              3 4 5 6 7 8 P   1 2 3 4 5 6 Q   7 8 1 2 3 4     5 6 7 8 1 2 R   3 4 5 6 7 8 P

RECEIVER:

R
(=R104)                     R R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R
                            1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2

I
(=I109)                     #SR . . . . . . . #SP . . . . . . . #SQ . . . . . . #SR .

IA
(=Q106)                                                       #
```

7Z24947

→ time

Notes

*   sample moment of the interchange circuit
#   change point of the interchange circuit

Fig.B2 Sample moments and change points of the interchange circuit C, CA, IA and I using a 4-byte frame (REC. X.30).
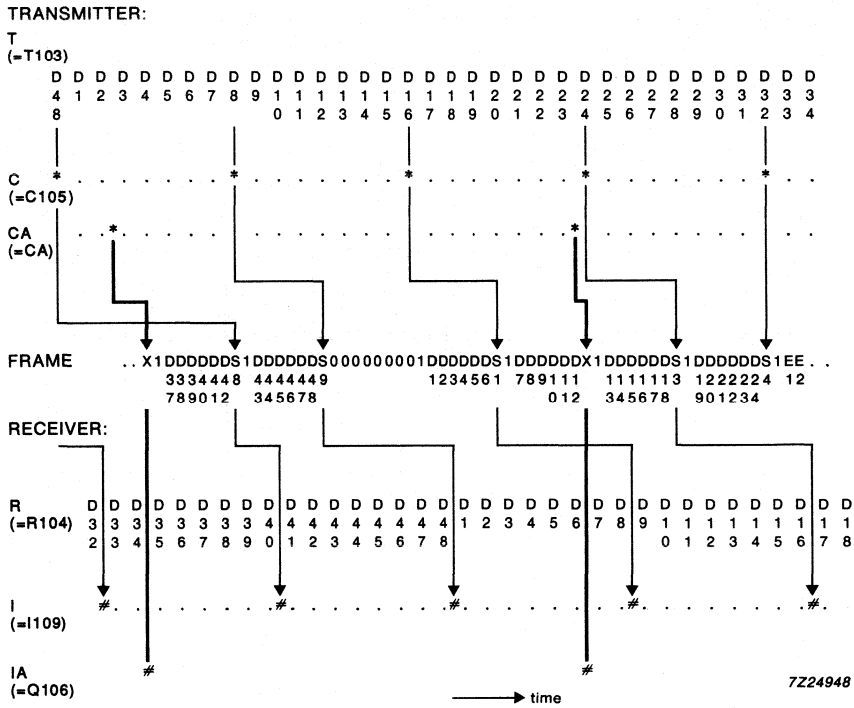
DEVELOPMENT DATA

TRANSMITTER:

T
(=T103)

C
(=C105)

CA
(=CA)

FRAME

RECEIVER:

R
(=R104)

I
(=I109)

IA
(=Q106)

7Z24948

→ time

Notes

*   sample moment of the interchange circuit
#   change point of the interchange circuit

When bit repetition is used (600, 1200 and 2400 bits/s) the value of the last sample of the interchange circuits is repeated in the 'S' and 'X' data bits until a new sample is made (see Appendix A Tables A2, A3 and A4).

Fig.B3 Sample moments and change points of the interchange circuit 105, CA, 106 and 109 using a 10-byte frame (REC. V.110).

TRANSMITTER:
T
(=T103)

```
          D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D
          1 1 1 1 2 2 2 2 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 2 2 2 2 1 2
          6 7 8 9 0 1 2 3                 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4
```

C
(=C105)   . . . . * . . . . * . . . . * . . . . * .

CA
(=CA)   *

FRAME   . . . 1 DDDDDDS 1 DDDDDDS 0 DDDDDDX 1 DDDDDDS 1 DDDDDDS 1 . . .
                      1222224   1234561   789111   1111113   1222224
RECEIVER: 901234   012   345678   901234

R
(=R104)

```
          D D D D D D D D D D D D D D D D D D D D D D D D
          1 1 1 2 2 2 2 2 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1
          7 8 9 0 1 2 3 4                 0 1 2 3 4 5 6 7 8
```

I
(=I109)   #. . . . . #. . . . . #. . . . .#. .

IA
(=Q106)   #   7Z24949

─────▶ time

Notes

* sample moment of the interchange circuit
# change point of the interchange circuit

Fig.B4 Sample moments and change points of the interchange circuit 105, CA, 106 and 109 using a 4-byte frame (REC. V.110).

Specification of the PCB2325
Extended Data Rate Adapter

Extended data rate adaptor   PCB2325

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Extended data rate adaptor   PCB2325

Extended data rate adaptor   PCB2325

1. Introduction

The Extended Data Rate Adapter (EDRA) is a CMOS integrated circuit for ISDN applications developed to adapt synchonous and asynchronous user data rates on the CCITT R-interface to a 64 kbit/s data stream and vice versa.

1.1. Features

* Data rate adaption to 64 kbit/s according CCITT V.110/X.30 and ECMA-102 recommendations.

* Synchronous data rates supported:

600, 1200, 2400, 4800, 9600, 19200, 38400, 48000, 56000 and 64000 bit/s.

* Asynchronous data rates supported (using RAO asynchronous-synchronous conversion):

full duplex with the same rates:

300, 600, 1200, 2400, 4800, 9600, 19200

or full duplex with:

1200/75 and 75/1200 bit/s.

* Asynchronous automatic data rate adaption from 0 upto 19.2 kbit/s using a multiple sampling method with additional transition coding (based on CCITT rec. R.111), for compatibility with its predecessor the PCB2320 DRA. Useful for data rates as:

50, 75, 110, 134.5, 150, 200, 3600, 7200, 12000, 14400 and 19200 bit/s.

* Flexible synchronous data interface, which supports both long and short frame synchronisation, i.e. connectable to:

     -2.048 Mbit/s Terminal highway;
     -SLD interface;
     -IOM interface (not in MPX mode);

* Submultiplexing, according to CCITT rec. I.460, permits upto 8 EDRAs to share one 64 kbit/s channel on the synchronous data interface.

* Serial interface for the DTE/DCE. A complete set of V- or X-series interchange circuits is supported.

* Microcontroller interface with multiplexed data/address lines.

* Built in UART for microcontroller access to both local and remote side of the data channel.

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* Local flowcontrol by control of lead 106 or X-ON/X-OFF.

* End to end flowcontrol.

* Inband Parameter Exchange (IPE), according to ECMA-102 recommendation:
  - unrestricted 64 kbit/s;
  - restricted 56 kbit/s;
  - asynchronous RA0;
  - asynchronous multiple-sampling.

* Network Independent Clocking (NIC) (for synchronous data rates), according
to CCITT rec. V.110 and ECMA-102, for the data rates of:

4800, 9600 and 19200 bit/s.

* Automatic speed recognition with aid of the microcontroller for data rates
upto 19.2 kbit/s.

* EDRA is usable in an interrupt driven environment (open drain interrupt
output).

* Monitoring and clamping of the interchange circuits (by microcontroller).

* Low power (power consumption < 40 mW).

* Powerdown mode (power consumption in powerdown mode < 0.2 mW).

* Maintenance loops.

* Boundary scan test.

* Single 5V supply power.

1.2. Ordering information

TYPE NUMBER	TEMPERATURE RANGE $^\circ$C	PACKAGE
PCB2325	-10 .. 75°C	PLCC 44
PCB2325	-10 .. 75°C	DIL 40

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1.3. <u>Signal description</u>

1.3.1. <u>PLCC 44 package</u>

```
              MCLK  BSC    VDD   BSI   C105
         RDN    SCLK   SCC    BSE   T103  R104

            6   5   4   3   2   1   44  43  42  41  40
   WRN ——   7                                      39   —— DCE106
   DB0 ——   8                                      38   —— DTE106
   DB1 ——   9                                      37   —— S114
   DB2 ——  10                                      36   —— MI2
   VSS ——  11              EDRA                     35   —— MI1
   nc  ——  12            (top view)                 34   —— nc
   DB3 ——  13                                      33   —— VDD
   DB4 ——  14                                      32   —— I109
   DB5 ——  15                                      31   —— V107
   DB6 ——  16                                      30   —— V108
   DB7 ——  17                                      29   —— MO2
           18  19  20  21  22  23  24  25  26  27  28

      CSN     ALE     SDO     FSR     B115  MO1
         INTN    FSX     VDD     SDI     S113
```
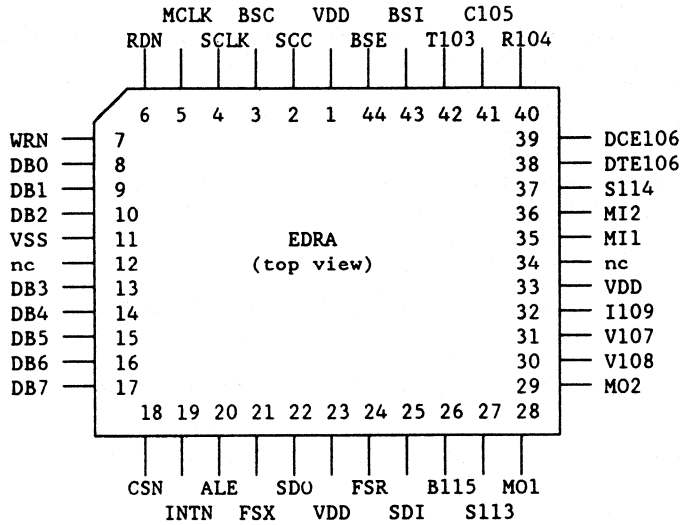
Figure 1.3-1 Pinning diagram (PLCC 44)

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1.3.2. <u>DIL 40 package</u>

```
        SCC ──┤ 1        40 ├── BSE
        BSC ──┤ 2        39 ├── BSI
       SCLK ──┤ 3        38 ├── T103
       MCLK ──┤ 4        37 ├── C105
        RDN ──┤ 5        36 ├── R104
        WRN ──┤ 6        35 ├── DCE106
        DB0 ──┤ 7        34 ├── DTE106
        DB1 ──┤ 8        33 ├── S114
        DB2 ──┤ 9        32 ├── MI2
        VSS ──┤ 10  EDRA 31 ├── MI1
        DB3 ──┤ 11       30 ├── VDD
        DB4 ──┤ 12       29 ├── I109
        DB5 ──┤ 13       28 ├── V107
        DB6 ──┤ 14       27 ├── V108
        DB7 ──┤ 15       26 ├── MO2
        CSN ──┤ 16       25 ├── MO1
       INTN ──┤ 17       24 ├── S113
        ALE ──┤ 18       23 ├── B115
        FSX ──┤ 19       22 ├── SDI
        SDO ──┤ 20       21 ├── FSR
```
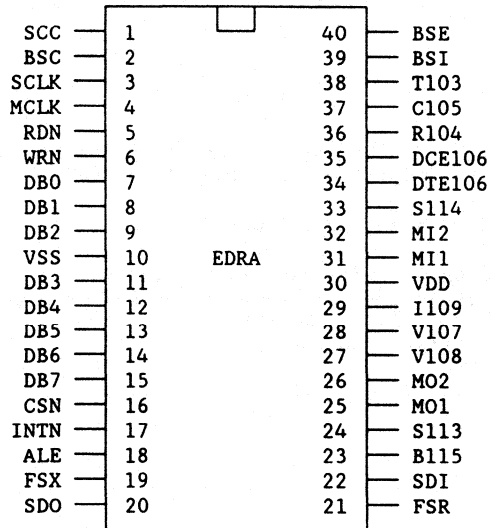
Figure 1.3-2 Pinning diagram (DIL 40)

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The signals names which are illustrated in figure 1.3-1 and figure 1.3-2
are now described. The pin numbers refer to the PLCC 44 package (figure 1.3-1) and the pin numbers between brackets refer to the DIL 40 package (figure 1.3-2).

1   VDD   Power supply connection +5V.

2 (1)   SCC   Scan Control input. Together with BSI (pin 43 (39)) and BSE
                (pin 44 (40)) the test-mode of the EDRA is determined.

3 (2)   BSC   Boundary scan clock input.

4 (3)   SCLK   Synchronous interface clock input (64 kHz - 2.048 MHz). SCLK
                determines the data rate on the synchronous data interface.

5 (4)   MCLK   Master clock input (2.048 MHz).

6 (5)   RDN   Read Not input (active low). Data is set on the μC-bus by
                EDRA (if selected by CSN), after the trailing edge of RDN.

7 (6)   WRN   Write Not input (active low). The μC writes data into the
                EDRA (if selected by CSN). Data is latched on the leading
                edge of WRN.

8 (7)   DB0   Data/address line 0 (LSB).

9 (8)   DB1   Data/address line 1.

10 (9)   DB2   Data/address line 2.

11 (10) VSS   Ground

12   n.c.   Not connected

13 (11) DB3   Data/address line 3.

14 (12) DB4   Data/address line 4.

15 (13) DB5   Data/address line 5.

16 (14) DB6   Data/address line 6.

17 (15) DB7   Data/address line 7 (MSB).

18 (16) CSN   Chip Select input (active low).

19 (17) INTN   Interrupt output (active low, open drain).

20 (18) ALE   Address Latch Enable input. Indicates that the combined
                data/address bus contains an address.

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21 (19)   FSX   Transmit Frame Select input. FSX aligns every 125 μs the 8 data bits on SDO (pin 22 (20)).

22 (20)   SDO   Synchronous Data output. Data output of the synchronous data interface.

23   VDD   Power supply connection +5V.

24 (21)   FSR   Receive Frame Select input. FSR aligns every 125 μs the 8 data bits for the EDRA on SDI (pin 25 (22)).

25 (22)   SDI   Synchronous data input. Serial data input of the synchronous data interface.

26 (23)   B115   Byte timing (B) or receiver element timing output. Signal B is a CCITT X-series defined control signal. This circuit provides the DTE the byte timing signal. The output pin B indicates the last bit of a data-byte. It will be HIGH during one period of S114 (pin 37 (33)) and will be LOW within the byte-period.

                     Receiver element timing output. Circuit 115 (V-series) generates the data element clock for circuit R104 (pin 40 (36)).

27 (24)   S113   Transmitter element timing input (provided by the DTE). S113 provides the data element timing for T103 (pin 42 (38)).

28 (25)   MO1   Multifunctional output 1.

29 (26)   MO2   Multifunctional output 2.

30 (27)   V108   Data Terminal Ready input. Indicates that the associated terminal is ready to receive and transmit data.

31 (28)   V107   Data Set Ready output. Indicates that to the terminal that the EDRA is ready to receive data. Output V107 indicates the state of the remote subscribers V108 circuit.

32 (29)   I109   Data channel received line signal detector/indication. Output which indicates the state of the remote subscribers C105 circuit. Under control of the μC, I109 can be made byte-timing synchronous. This pin is in boundary test mode boundary scan output.

33 (30)   VDD   Power supply connection +5V.

34   n.c.   Not connected.

35 (31)   MI1   Multifunctional input 1.

36 (32)   MI2   Multifunctional input 2.

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37 (33) S114 Transmitter element timing output. In synchronous mode S114 generates the data element clock for circuit T103 (pin 42 (38)).

38 (34) DTE106 Request To Send input (EDRA=DTE).

39 (35) DCE106 Request To Send output. Output which indicates the state of the remote subscribers DTE106 circuit.

40 (36) R104 Received data output. R104 provides circuit 104 for V- and R for X-series of interfaces. Circuit R104 will be shifted out every trailing edge of S114 (pin 37 (33)).

41 (37) C105 For V-series, C105 performs as circuit 105, for X-series as circuit C. C105 is a signalling channel which corresponds with I109 of the remote subscriber.

42 (38) T103 Transmit data input. Transmit input has to be connected to the transmit (T for X-, circuit 103 for V-series) output of the DTE equipment. For synchronous speeds T103 will be sampled at every leading edge of B115 (pin 26 (23)).

43 (39) BSI Boundary scan input.

44 (40) BSE Boundary scan enable.

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2. Functional description

2.1. General description

The EDRA adapts synchronous and asynchronous user data rates on the so called R-interface fully in accordance to CCITT rec. X.30/V.110 and ECMA-102 recommendations to a 64 kbit/s channel (ISDN B-channel) and vice versa.

To be compatible with the EDRAs predecessor, the PCB2320 Data Rate Adapter (DRA) also multiple sampling is used. Asynchronous user data rates from 0 upto 19.2 kbit/s on the R-interface are also supported using the multiple sampling method with additional transition coding based on CCITT rec. R.111. With this multiple sampling method it is possible to convert every asynchronous user data rate to a 64 kbit/s data stream without the need of programming the EDRA for the specific user data rate of the DTE.

Network independent clocking is supported by the EDRA. It allows the EDRA to be connected to a synchronous modem with a data rate upto 19.2 kbit/s not locked to the user data rate of the EDRA without loss of data.

In order to provide a means to transfer data by μC to the remote EDRA, an IPE exchange mode is implemented. In this mode the μC can access the 64 kbit/s channel to transmit data to and receive data from the remote EDRA.

To be able to communicate with the DTE the μC connected to the EDRA can be connected to the R-interface. In this way the μC can demand the DTE for call setup information.

The conversion between user data rates and the 64 kbit/s data rate takes place RA0, RA1 and RA2 adaption stages as decribed in the CCITT X.30 and V.110 and ECMA-102 recommendations. The RA0 adaption stage performs the asynchronous-synchronous conversion, while the RA1 and RA2 adaption stage perform the conversion between a synchronous data rate (or synchronous data from the RA0 stage) to 64 kbit/s. In figure 2.1-1 a survey is given of the different data paths within the EDRA.

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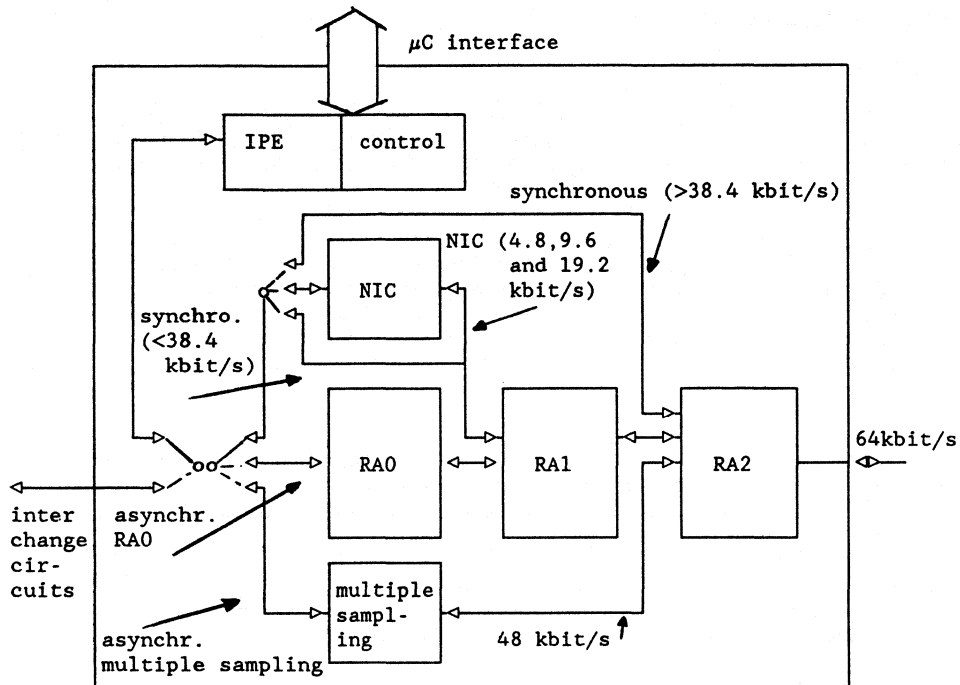
Figure 2.1-1 Data paths within the EDRA

In the EDRA different functional blocks can be distinghuised. These blocks
are illustrated in blockdiagram 2.1-2.

A brief description of the interfaces of the EDRA is given before the
functional blocks are described. In blockdiagram 2.1-2 three interfaces can
be destinguished:

*The interchange interface. A set of V-type interchange circuits: 103, 104,
105, 106, 107, 108, 109, 113, 114, 115 and two multifunctional input and two
multifunctional outputs or X-type data interface interchange circuits: T, R,
C, I, S and B can be connected to the EDRA via level converters. This
interchange interface is described in section 2.3.

*The synchronous data interface can have a transmission rate between 64
kbit/s and 2.048 Mbit/s. The interface consists of two unidirectional data
lines (SDI and SDO), a clock line (SCLK) determining the transmission rate
on this interface, a frame select transmit signal (FSX) and frame select
receive signal (FSR) which indicate the transmit and receive timeslot on the
synchronous data interface. The synchronous data interface is described in
section 2.4.

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interchange
circuits

MCLK

EDRA

T103				
C105		NIC		
DTE106		transmitter		
V108	IC-I		FM-	SDO
MI1		URF receiver	MS	
MI2				
S113		IPE transmitter		

CLOCKGENERATOR

SYNCHRO-CIRCUIT

SCLK
FSR
FSX

R104		NIC receiver		
DCE106				
V107		URF		
I109	IC-O	transmitter	FD-	SDI
MO1			MS	
MO2				
S114		IPE		
B115		receiver		

synchronous
data
interface

VDD
VSS

μC INTERFACE

ALE DB0-DB7 RDN WRN CSN INTN

microcontroller interface
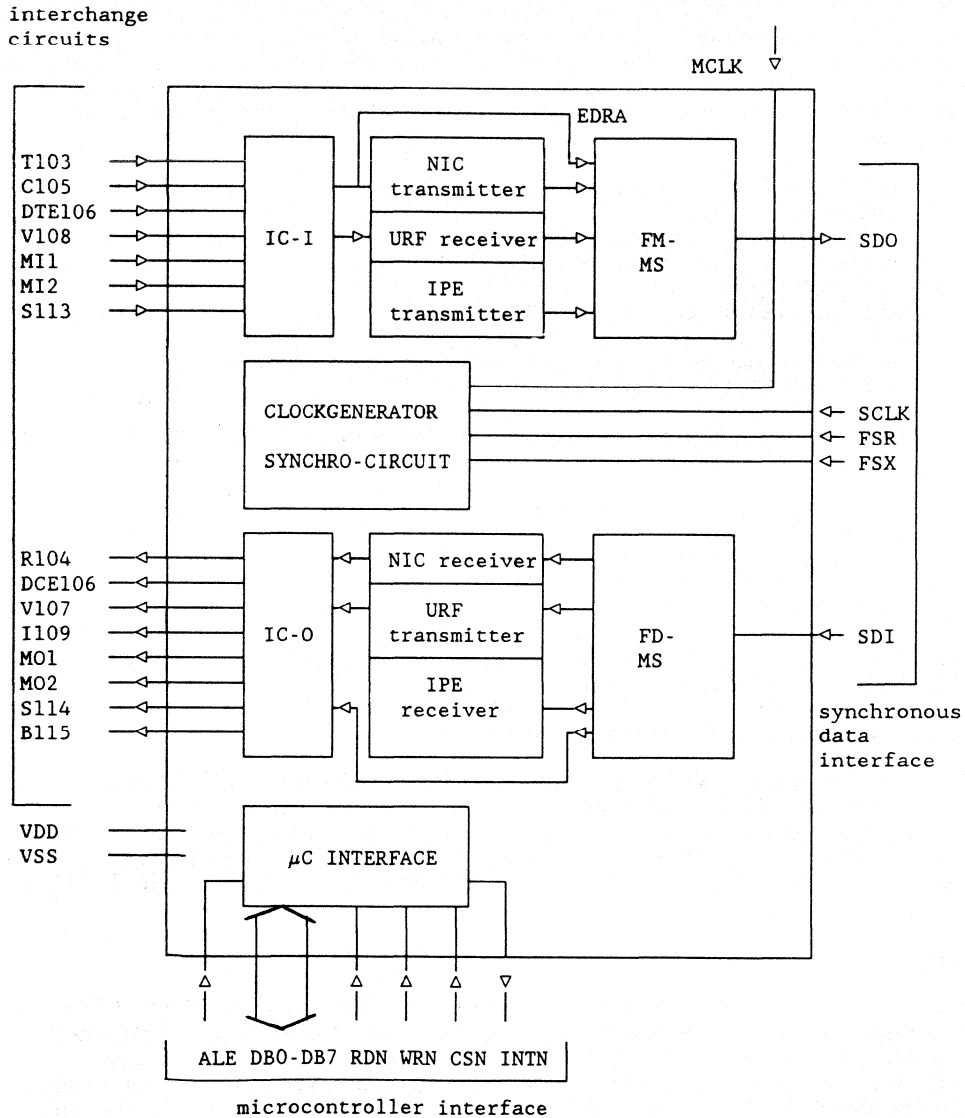
All the blocks in the EDRA are controlled via the μC interface and receive
their timing from the clock generator/synchronisation circuit.

Figure 2.1-2 Block diagram of the EDRA.

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*The 8 bit microcontroller interface is a data/address multiplexed
microcontroller interface. The microcontroller interface performs the
interface for the control stages of the EDRA. The EDRA can be programmed and
monitored via the microcontroller interface. The settings of the EDRA can be
programmed in a set of write registers. The following settings can be
programmed:

- selection of functional mode
- data rate setting
- the mapping scheme (interchange circuits to S- and X-bits)
- clamping of interchange circuits
- testloop selection
- communications control via UART
- interrupt masking
- 64 kbit/s channel framing and synchronisation control
- setting UART/flow control parameters

The EDRA can be monitored by reading out the read registers. The following
functions can be read out:

- in/out synchronisation-indication
- activity check on interchange circuits
- readout logic state of interchange circuits.
- readout of the interrupt source.
- readout the UART

The microcontroller interface description and the detailed description of
the registers is provided in section 2.9.

*Clock generator and synchronisation circuit

The clock generator and synchronisation circuit provides all internal
clocks of the EDRA. It generates i.e. the baud rates on circuits S114 and
115 and provides byte timing on circuit B. (B and 115 are physically one
circuit, but can be switched by the microcontroller). The baudrate on the
interchange interface can be selected with register W01, see section
2.9.1.2.

*Interchange circuits (inputs/outputs) (IC-I/IC-O)

The interchange circuit (input and output) blocks (IC-I and IC-O) interface
with the connected data equipment. All interchange circuits can be monitored
via the μC-interface. Via this block, the mapping of the interchange
circuits to the S- and X-bits in the frame on the synchronous data interface
can be chosen. A detailed desciption of these blocks is given in section
2.3.

*Frame mapping and demapping block and multiple-sampling coding/decoding
(FM-MS/FD-MS)

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The translation between synchronous user data rates and the 64 kbit/s
channel takes place in the frame mapping block (FM in figure 2.1-2) while
the reverse action is performed by the frame demapping block (FD). These
blocks perform the RA1 and RA2 stages as described in CCITT rec. X.30/V.110
and ECMA-102. The asynchronous to synchronous conversion according to the
multiple sampling method with additional transition coding is also performed
in the frame mapping/demapping block. A detailed description of the frame
mapping/demapping block is given in section 2.8.

*URF transmitter/receiver

URF transmitter/receiver block is a combination of three functions, UART,
RA0 adaption stage (according ECMA-102 and CCITT rec. V.22), flow-control
(FLC). A detailed description of the URF transmitter/receiver is given in
section 2.5.

*IPE transmitter/receiver

The Inband Parameter Exchange (IPE) function is discussed in 2.6.

*Network independent clocking transmitter/receiver

The NIC block allows the EDRA to be connected to a synchronous modem with a
data rate of 4800, 9600 or 19.2 kbit/s. A detailed description of the NIC
function is given in section 2.7.

2.2. Modes of operation

The EDRA can be used in three different modes of operation (illustrated in
figure 2.2-1) which can be programmed by the microcontroller:

* Transmission-mode 1: Local DTE to remote DTE.

    -1A: synchronous, data rate adaption according to CCITT rec. V.110 or
             X.30 (V.110 (asynchronous or bit synchronous) or X.30 mode
             (byte-synchronous) can be selected);
    -1B: asynchronous with the RA0 coding;
    -1C: asynchronous with flow control;
    -1D: asynchronous with multiple sampling and additional transition
             coding. In this mode the break character can be filtered out by
             microcontroller and user data can be read out via the
             microcontroller interface.

* Transmission-mode 2: Local DTE to local microcontroller.

    In this mode, the microcontroller can communicate to the DTE/DCE via
    the UART. Only asynchronous transmission is possible. the URF will
    be used as asynchronous receiver transmitter (the UART function).

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* Transmission-mode 3: Local microcontroller to 64 kbit/s channel.

  -3A: asynchronous, the 64 kbit/s channel data will be coded according
       the multiple sampling method. the URF will be used as
       asynchronous receiver transmitter (the UART function);
  -3B: asynchronous, IPE mode with RA0 coded data in 64 kbit/s channel.
       the URF will be used as asynchronous receiver transmitter (the
       UART function);
  -3C: synchronous, IPE mode with 64 or 56 kbit/s data rate in the 64
       kbit/s channel, The microcontroller uses the UART for
       parallel-serial conversion and the data in the 64 kbit/s channel
       will be coded according to the selected mode (56 or 64 kbit/s).
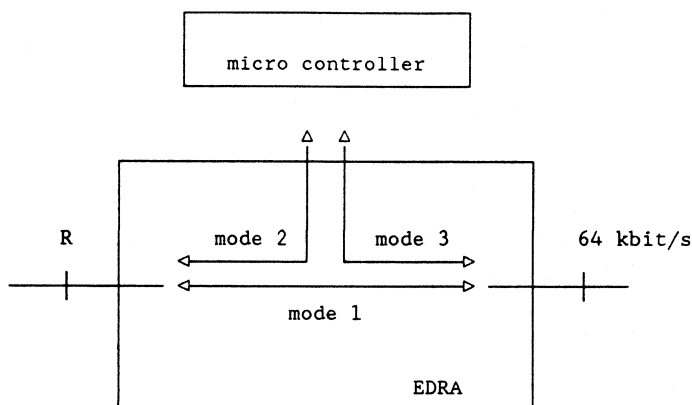
Figure 2.2-1 The three transmission modes of the EDRA

2.3. Interchange circuits

The interchange interface of the EDRA connects to level converters which
then connect to the DTE (or DCE) (see figure 2.3-1). The interchange
interface consists of:

*T103   :Circuit 103 (V-series), Transmitted Data.
              T (X-series), Transmit.

*R104   :Circuit 104 (V-series), Received Data.
              R (X-series), Receive.

*C105   :Circuit 105 (V-series), Request To Send.
              C (X-series), Control.

*DTE106   :Circuit 106 (V-series), Clear To Send (the EDRA is DTE).

*DCE106   :Circuit 106 (V-series), Clear To Send (the EDRA is DCE).

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*V107   :Circuit 107 (V-series), Data Set Ready.

*V108   :Circuit 108 (V-series), Data Terminal Ready.

*I109   :Circuit 109 (V-series), Data channel received line signal
             detector.
             I (X-series), Indication.

*S113   :Circuit 113 (V-series), Transmit signal element timing (from
             DTE).
             S (X-series), Signal element timing.

*S114   :Circuit 114 (V-series), Transmit signal element timing (from
             DCE).
             S (x-series), Signal element timing.

*B115   :Circuit 115 (V-series), Receiver signal element timing.
             B (X-series), Byte timing.

*MO1   :Multifunctional output 1.

*MO2   :Multifunctional output 2.

*MI1   :Multifunctional input 1.

*MI2   :Multifunctional input 2.

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```
R-interface
(V.28 level)                                 interchange interface

X | V    LA(level adaption)

T | 103                                  ▷   T103
C | 105                                  ▷   C105
- | 106                                  ▷   DTE106
- | 108                                  ▷   V108
- | x                                    ▷   OI1
- | x                                    ▷   OI2

S | 113                                  ▷   S113
S | 114                                  ◁   S114
- | 115                                  ◁   B115      EDRA
B | -

R | 104                                  ◁   R104
I | 109                                  ◁   I109
- | 106                                  ◁   DCE106
- | 107                                  ◁   V107
- | x                                    ◁   PO1
- | x                                    ◁   PO2
```
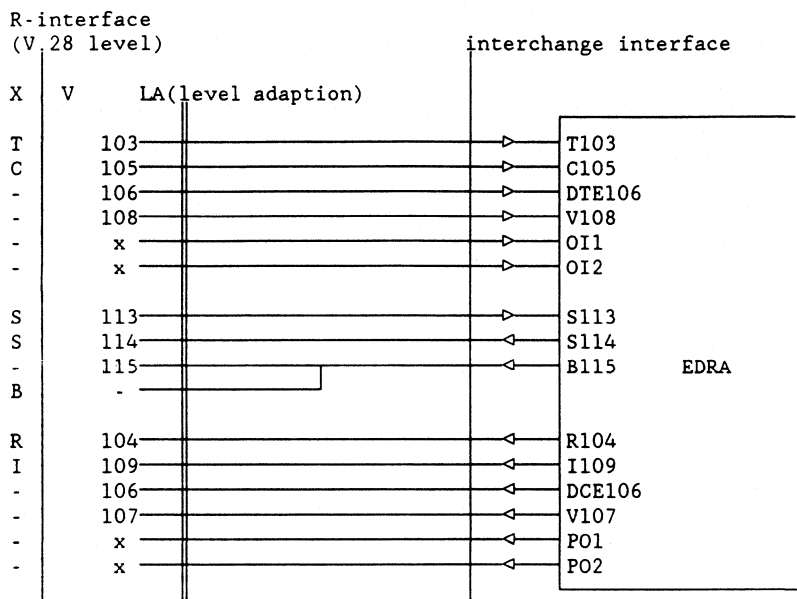
Figure 2.3-1 The interchange interface.

2.3.1. <u>Mapping of the interchange circuits in Data, S- and X-bits</u>

ECMA and CCITT specify the interchange circuits that should be mapped into
the frame used in the 64 kbit/s channel. In the EDRA the mapping of
interchange circuits into the 64 kbit/s channel can be performed in three
ways (see register W00, section 2.9.1.1):

-V.110 mode: in this mode the EDRA is asynchronous or bit synchronous but
not byte synchronous (see section 2.3.3).
-X.30 mode: in this mode the EDRA is byte synchronous (see section 2.3.3).

-μC mode: in this mode the S- and X-bits in the frame can be set and read by
μC.

For user data rates $\leq$ 38.4 kbit/s a 10 bytes multiframe is used (see
section 2.8.2 and appendix B for the description of this frame). Table
2.3.1-1 shows the mapping of interchange circuits in the bits of the
10-bytes multiframe.

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	local subscriber	frame bits	remote subscriber
V.110 mode	V108 C105 frame sync/DTE106 T103	S1,S3,S6,S8 S4,S9 X2,X7 D1 - D48	V107 I109 DCE106 R104
X.30 mode	C105 frame sync/DTE106 T103	SP, SQ, SR X2, X7 P1 - R8	I109 DCE106 R104
μC-mode	register W07	S1,X2,S3,S4,S6,X7, S8,S9	register R24 (bit 0-7)

Table 2.3.1-1 Mapping of interchange circuits for user data rates $\leq$ 38.4 kbit/s.

For the user data rate of 48 kbit/s a four bytes frame is used (see section 2.8.2 and appendix B for the description of this frame). In table 2.3.1-2 the mapping of the interchange circuits in the bits of the 4 bytes frame is illustrated.

For a user data rate of 56 kbit/s only one S-bit is available (in the 4 bytes frame) to transmit one interchange circuit. The mapping of the interchange circuits for the user data rate of 56 kbit/s is illustrated in table 2.3.1-3 (see section 2.8.2 and appendix B for a description of this frame).

	local subscriber	frame bits	remote subscriber
V.110 mode	V108 C105 frame sync/DTE106 T103	S1,S3 S4 X2 D1 - D24	V107 I109 DCE106 R104
X.30 mode	C105 frame sync/DTE106 T103	SP, SQ, SR X2 P1 - R8	I109 DCE106 R104
μC-mode	register W07 (S6-S9 not relevant)	S1,X2,S3,S4	register R24 (bit 0-3)

Table 2.3.1-2 Mapping of interchange circuits for a user data rate of 48 kbit/s.

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	local subscriber	frame bits	remote subscriber
X.30 mode	C105 T103	S D1 - D28	I109 R104
μC-mode	the S bit wil not be influenced by W07 in the μC-mode, the S bit is directly coupled to lead C105. clamping of C105	S	register R24, bit 0

Table 2.3.1-3 Mapping of interchange circuits for a user data rate of 56
           kbit/s.

2.3.2. Relation between ON/OFF and their binary values

In the december '84 ECMA specification, the binary values of S- and X-bits
in the data stream on the synchronous data interface are given related to ON
or OFF conditions of the interchange circuits:

For the S- and X-bits, a zero corresponds with the ON condition, a one with
the OFF condition.

In the september '84 ECMA report this definition was reverse: zero
corresponds with OFF, a one with ON.

To meet both definitions (and so to be upwards compatible with the DRA),
both definitions can be selected in registers W5/W10 (section 2.9.1). When
the EDRA is connected to a DRA, the EDRA must code the S- and X-bits
according the september ECMA definition. When other networks are involved,
the EDRA must be V.110 compatible (december '84 ECMA definition) and can not
cooperate with the DRA anymore. In figure 2.3.2-1 the relation between the
signals on the interchange circuits and the signals on the EDRA pins are
depicted.

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Signal	V.28 level <= -3V	V.28 level >= 3V	comment
T103	1	0	Condition 0 on V.28 level = condition 0 in the data bits on the SD interface.
R104	1	0	Condition 1 on V.28 level = condition 1 in the data bits on the SD interface.
C105	OFF	ON	Condition ON on V.28 level = condition 0 in the S- and X-bits on the SD interface (V.110 mode).
DTE106	OFF	ON	Condition OFF on V.28 level = condition 1 in the S- and X-bits on the SD interface (V.110 mode).
DCE106	OFF	ON	
V107	OFF	ON	
V108	OFF	ON	Condition ON on V.28 level = condition 1 in the S- and X-bits on the SD interface (DRA-mode).
I109	OFF	ON	
S113	OFF	ON	
S114	OFF	ON	Condition OFF on V.28 level = condition 0 in the S- and X-bits on the SD interface (DRA-mode)
B115	OFF	ON	

Table 2.3.2-1 Relation between the signals on the interchange circuits and the signals on the EDRA.

2.3.3. Functional timing relations

In X.30 mode, the byte timing interchange circuit B is provided for character alignment (pin B115). Circuit C (pin C105) is sampled together with bit 8 of the preceeding character (on T103). The timing of the outgoing interchange circuits is related to this byte timing signal. Circuit I (pin I109) is changing its state at the boundaried between old and new character at circuit R (pin R104). In figure 2.3.3-1 the relation in timing between the interchange circuits is depicted. The receiver block provides byte- and bit-synchronisation, and delaying of circuits I and R, to fit the byte-timing for X.21 interfaces.

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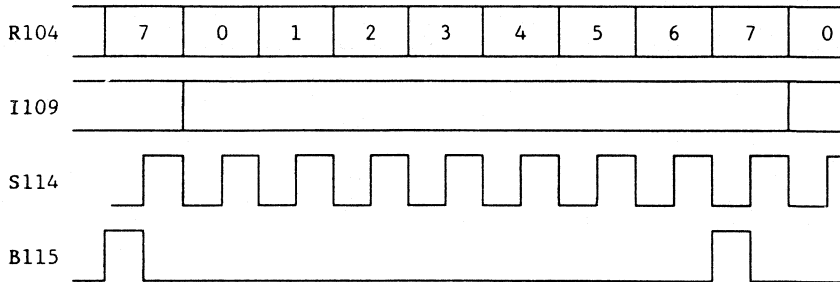
Figure 2.3.3-1 Byte timing relation between data and S bits.

In appendix A the sampling moments and the moment of state changes of the interchange circuits in X.30 mode are depicted for the 4 bytes frame and the 10 bytes multiframe (see also section 2.8.2).

In V.110 mode the receiver data (on pin R104) is not byte synchronous with the transmitter data (T103). The received S-bits are related to databits as follows depicted in table 2.3.3-2.

S-bit	D-bit
S1	D8
S3	D16
S4	D24
S6	D32
S8	D40
S9	D48

Table 2.3.3-2 Coordination of S-bits to D-bits.

In appendix A the sampling moments and the moment of state changes of the interchange circuits in V.110 mode are illustrated for the 4 bytes frame and the 10 bytes multiframe (see also section 2.8.2).

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2.4. Synchronous data interface

The synchronous data interface (illustrated in figure 2.4-1) consists of :

- SDI: Synchronous data input;
- SDO: Synchronous data output;
- SCLK: Data element clock (64 kHz - 2.048 MHz);
- FSR: Receive frame select;
- FSX: Transmit frame select.
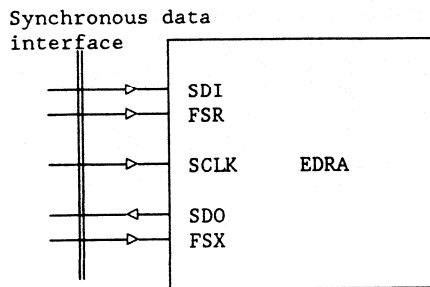
2.4-1 Synchronous data interface.

The synchronous data interface can operate between at a data rate between 64 kbit/s and 2.048 Mbit/s. The synchronous data interface operates in short synchronisation mode. However, a long synchronisation signal may be used if a minimal off-time Tw is taken into account (see figure 2.4.1-1 and section 3.3).
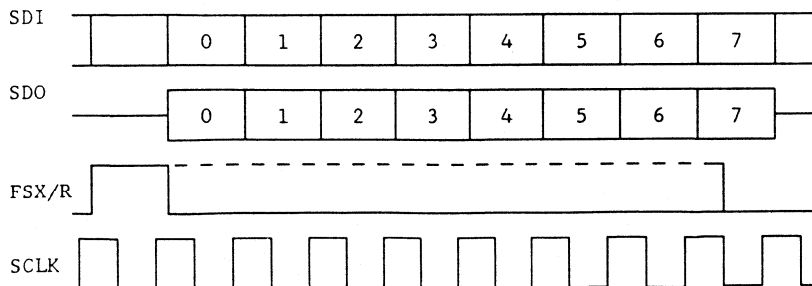
Figure 2.4.1-1 Synchronous data interface functional timing.

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The last data rate adaption stage, RA2, converts intermediate rates from
the RA1 adaption stage to the 64 kbit/s data rate (see section 2.8.2).
Instead of the adaption from the intermediate rate to the 64 kbit/s data
rate, the intermediate data rate can be placed in a part of the 64 kbit/s
channel of the synchronous data interface. This means that for an
intermediate rate of 8 kbit/s (user data upto 4.8 kbit/s) only the one of
the eight bits of the timeslot is used and eight EDRAs can be (time
division) multiplexed in one 64 kbit/s channel. For an intermediate rate of
16 kbit/s, four EDRAs can share the same 64 kbit/s channel and for an
intermediate rate of 32 kbit/s two EDRAs.

Via the microcontroller interface the selection of the bit position that
will be occupied in the 64 kbit/s bitstream can be chosen: an 8 kbit/s
intermediate bitstream may occupy any bit position, a 16 kbit/s intermediate
stream occupies bit positions (0,1) or (2,3) or (4,5) or (6,7), a 32 kbit/s
intermediate stream occupies bit positions (0,1,2,3) or (4,5,6,7); the bit
position selections can be made in register W03 (section 2.9.1.4).
The order of transmission of the bits at each intermediate rate will be
identical at transmitter and receiver. The highway output will 3-state all
unused bits, this to enable another EDRA to transmit data in the same
timeslot on the synchronous data interface.

2.5. URF transmitter/receiver

URF transmitter/receiver performs three functions, UART, RA0, flow-control
(FLC). In figure 2.5-1 the URF transmitter/receiver block is illustrated.
In this figure the data streams for the different operational modes of the
EDRA (as discussed in section 2.2) are shown. In addition to figure 2.5-1
the URF transmitter and receiver are shown in more detail in figure 2.5-2
and figure 2.5-3. The different functions of the URF transmitter/receiver
are discussed in the following sections.

Extended data rate adaptor   PCB2325
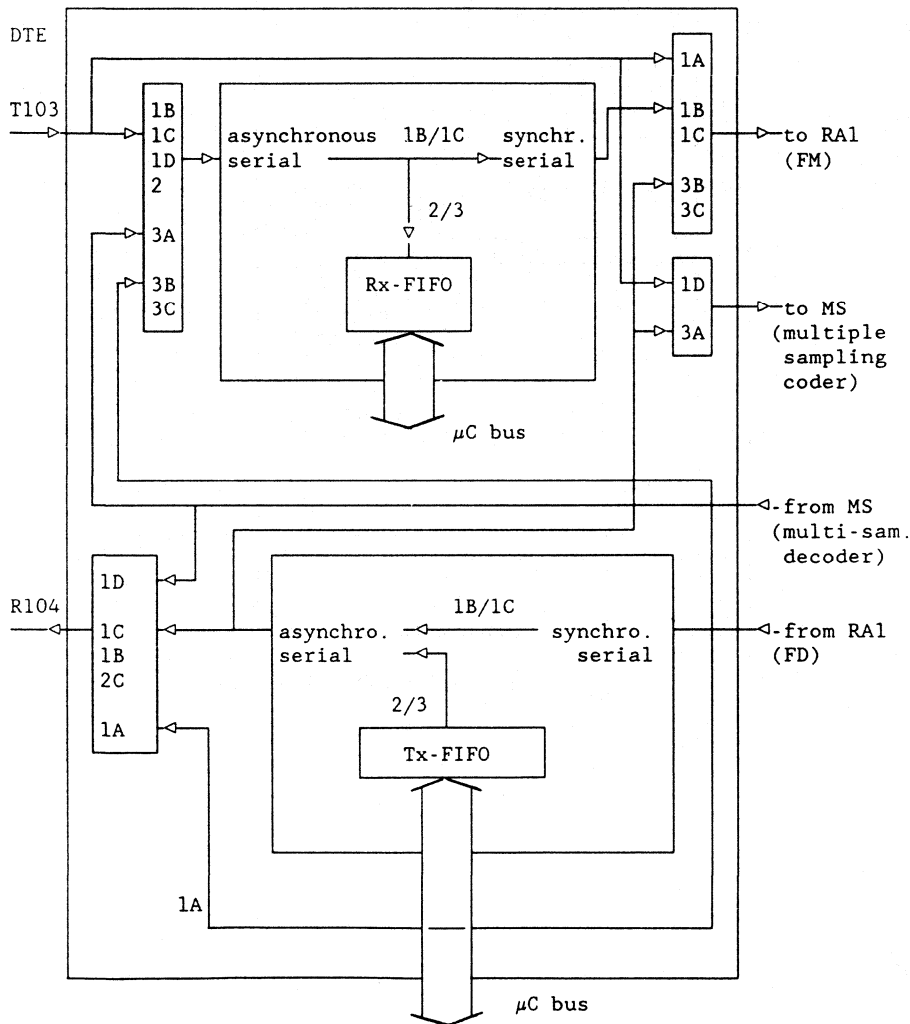
Figure 2.5-1 The URF transmitter/receiver.
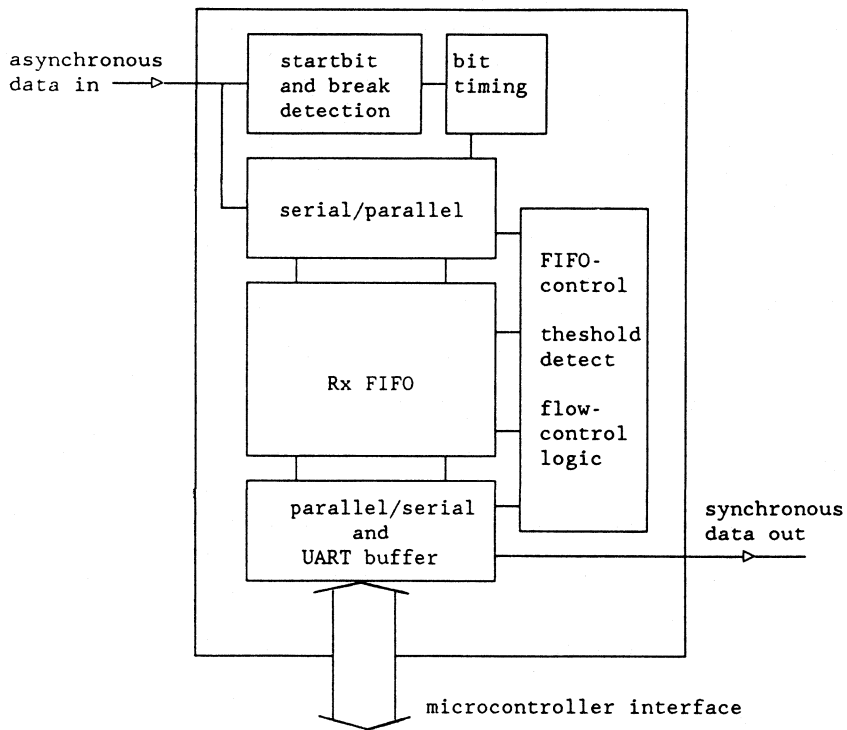
Figure 2.5-2 URF receiver

Extended data rate adaptor

PCB2325
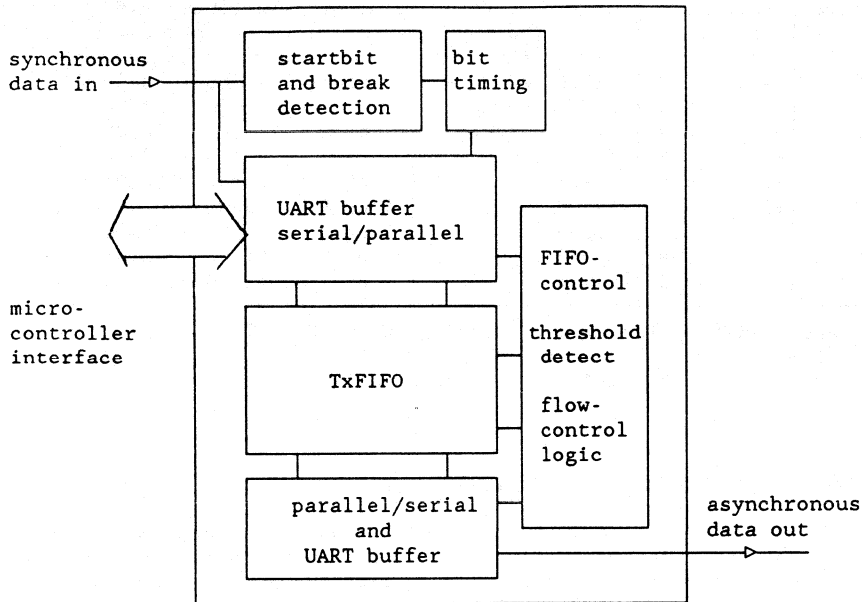
Figure 2.5-3 URF transmitter

2.5.1. RA0 converter

In transmission mode 1B, 1C and 3B the RA0 function is used. Function RA0 is an asynchronous to synchronous conversion stage (and vice versa), using the technique of ECMA-102/CCITT V.22. RA0 converts asynchronous user data to synchronous data of $2^{**}n * 600$ bit/s, where $n = [0,1,2,3,4,5]$ (speed setting by μC is needed). This will be done by adding stopbits to fit the nearest synchronous channel. In table 2.5.1-1 the supported speeds and their relations to synchronous- and intermediate rate are depicted.

Extended data rate adaptor   PCB2325

URF data-rate bps	rate tolerance % *	data bits	added parity	stop bits	possible FRAME speed selections
300	+4.8/ -4.8	5/7/8	odd/even/	1 or 2	600 - 38400
600	+1 / -4.8	5/7/8	none/	1 or 2	600 - 38400
1200	+1 / -4.8	5/7/8	mark/spac	1 or 2	1200 - 38400
2400	+1 / -4.8	5/7/8	,,	1 or 2	2400 - 38400
4800	+1 / -4.8	5/7/8	,,	1 or 2	4800 - 38400
9600	+1 / -4.8	5/7/8	,,	1 or 2	9600 - 38400
19200	+1 / -4.8	5/7/8	,,	1 or 2	19200 - 38400
1200/75	+1 / -4.8	5/7/8	,,	1 or 2	fixed 1200 bps
75/1200	+1 / -4.8	5/7/8	,,	1 or 2	fixed 1200 bps

* tolerances without Flowcontrol-setting. With FLC all tolerances are +/- 4.8 %

Table 2.5.1-1 Asynchronous data rates.

2.5.1.1. RA0 asynchronous to synchronous conversion

In this section the asynchronous to synchronous conversion algorithm performed by the RA0-function is discussed. The asynchronous to synchronous conversion takes place in two stages. In the first stage an asynchronous data byte is received and placed in the Rx-FIFO (illustrated in figure 2.5-2). In the second stage the data byte is taken out of the Rx-FIFO and transmitted synchronously.

The following actions are performed by the URF receiver for the conversion of asynchronous data (on pin T103) to the Rx-FIFO:

I1. detects a period of n stopbits. This is needed for character synchronisation.
I2. detects the trailing edge of the startbit.
I3. and starts counting to the middle of this bit (at frequency 16*baudrate), checks state zero. If not back to I1.
I4. starts latching incoming bitstream in a shift-in register
I5. increment bitcounter.
I6. at expected stopbit, checks of state one. If so, loads contents of shift-in register into the Rx-FIFO and goto I2.
I6a. If not and a null character has been shifted in, it loads a null character and gives a breaksignal. It waits until a rising edge of a stopbit, goto I2.
I6b. If no stopbit is present at the expected moment and no null character is received, it loads the shift in character into the Rx-FIFO and gives the frame-error signal and continues counting to the next expected middle of a databit, checks if this bit is a start- or a stopbit. If it is a stopbit goto I2. Otherwise goto I4.

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The following actions are performed to convert the data from the Rx-FIFO to
the synchronous data stream:

01. When a character is available in the Rx-FIFO, data is loaded into a
    shift-out register (parallel/serial and UART buffer block in figure
    2.5-2).
02. The shift-out register is clocked continuously with the used synchronous
    clock. After shifting out the parallel loaded Rx-FIFO information, the
    shift-out register continues sending ones (stopbits) until a character
    is available in the Rx-FIFO.

In figure 2.5.1.1-1 this procedure is illustrated for asynchronous user data
of 300 baud with 7 data bits, 1 start bit and 1 stopbit.

input signal (300 baud):

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

synchronous
outputsignal 600 bit/s:

2|3|4|5|6|7|8|8|8|8|8|8|8|8|8|8|0|1|2|3|4|5|6|7|8|8|8|8|8|8|8|8|8|8|

|<──────────────────────>|
T- inter character interval
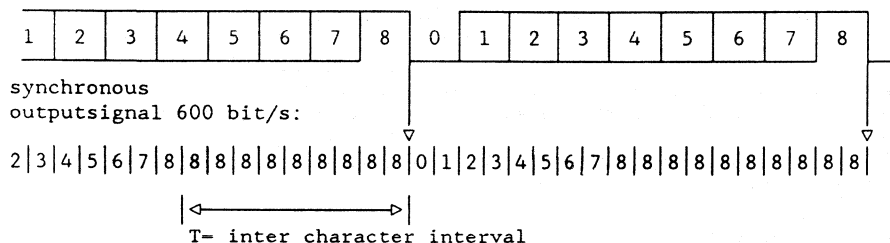
Figure 2.5.1.1-1 RA0 adaption of a 300 baud asynchronous user data rate.

In case the asynchronous user data has a baud rate that is a fraction
higher than the nominal baud rate (overspeed), the intervaltime T (figure
2.5.1.1-1) will become smaller because of the insertion of less stopbits.
This implies that at a certain user data rate the RA0-transmitter may
sometimes delete the only stopbit there is. This causes problems at the
remote DEDRA when the transmitted characters are sent with minimal spacing.

This problem is due to the RA0 method. In CCITT rec. V.110 and ECMA-102 the
following solution recommended: Because of the overspeed, the contents of
the Tx-FIFO (at the remote EDRA) is increasing. To prevent the FIFO to
overflow, the EDRA detects a fixed threshold level of the FIFO at two
characters. Now the stopbits of the asynchronous to be sent characters are
shortened to 7/8 of the normal length. In the case that two stopbits per
character are selected, only one stopbit is shortened.

If the baud rate of the user data is somewhat less than the nominal rate
(underspeed), the interval T may be longer than nominal because of an extra
insertion of a stopbit. This extra stopbit does not affect the transmission.

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2.5.1.2. <u>RAO synchronous to asynchronous conversion</u>

In this section the synchronous to asynchronous conversion by the RAO-function is discussed. The synchronous to asynchronous conversion takes place in two stages. In the first stage a synchronous data byte is received and placed in the Tx-FIFO. In the second stage the data byte is taken out of the Tx-FIFO and transmitted asynchronously (see figure 2.5-3).

The following actions are performed by the URF transmitter to convert synchronous data to the Tx-FIFO:

I1. It starts up with a longer period of stopelements.
I2. searches for the startbit; samples the received synchronous bitstream on the S114 falling edge. The first detected zero is the startbit.
I3. shifts the following characterbits in a shiftin register.
I4. when the whole character is shifted in, the character wil be loaded into the Tx-FIFO, and goto I2.

The following actions are performed to transfer data from from Tx-FIFO to the asynchronous user data stream (R104 output):

O1. until a character is available in the Tx-FIFO, it will transmit stopbits.
O2. loads the character into the shift-out register including a startbit and the selected number of stopbits. In case that the fixed threshold is reached, one stopbit is shortened to 7/8. After this go back to O1.

For 1% overspeed, maximum once per eight characters, a stop-element will be deleted.

2.5.1.3. <u>Break signal detection</u>

RAO asynchronous to synchronous converter is able to detect a break signal (continuous zeros on input T103) of the DTE connected to the EDRA. If the RAO converter detects M to 2M+3 bits, all of start polarity (zero), where M is the number of bits per character in the selected format including start-, parity- and stopbits, RAO transmits 2M+3 bits of start polarity (at the synchronous speed). If RAO detects more than 2M+3 bits of start polarity, it transmits all these bits as start polarity.

M = nr. of databits + paritybit + startbit + stopbits.

Note:

The DTE must transmit on circuit 103 at least 2M bits of stop polarity after the start polarity break signal, before sending further data characters. The RAO converter will then be able to regain character synchronisation from the following stop/start transition, else character synchronisation may be lost. This fully in accordance to CCITT rec. V.110.

If 2M+3 or more bits of start polarity are received from the remote EDRA these bits are output to the DTE connected to the EDRA.

In figure 2.5.1.3-1 the transmission of the break signal is illustrated:
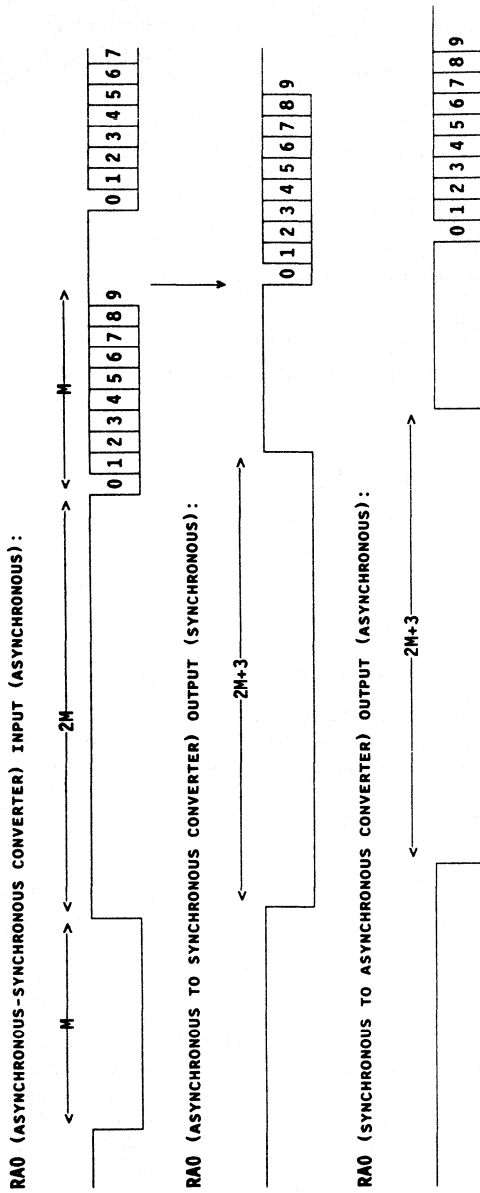
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RA0 (ASYNCHRONOUS-SYNCHRONOUS CONVERTER) INPUT (ASYNCHRONOUS):

RA0 (ASYNCHRONOUS TO SYNCHRONOUS CONVERTER) OUTPUT (SYNCHRONOUS):

RA0 (SYNCHRONOUS TO ASYNCHRONOUS CONVERTER) OUTPUT (ASYNCHRONOUS):

NOTE: M=10, 1 START BIT, 7 DATABITS, 1 PARITY BIT AND 1 STOP BIT.

Figure 2.5.1.3-1 the transmission of the break signal

2.5.2. UART

The UART is used in transmission mode 2 of the EDRA. It is also used in
transmission mode 1B, 1C, 3A, 3B, 3C to do the serial parallel conversion
(and vice versa) as was discussed in section 2.5.1. In mode 1D the UART can
be used to monitor the data from the DTE.

The UART that is part of the URF transmitter/receiver has the following
capabilities:

- Receive buffer: 32 bytes FIFO.
- Transmit buffer: 32 bytes FIFO.
- Threshold levels for FIFO guarding are programmable (for different
  flow control situations).
- Split speeds 1200/75 only.
- All registers directly addressable.
- Receiver and transmit interrupt indication in general interrupt
  status register.
- 5/7/8 bits/char excluding parity.
- number of stop bits: one or two.
- odd, even ,mark ,space or no parity.
- break generation and detection.
- parity, overrun and framing error detection.
- Two basic I/O modes are supported: polling and interrupt driven.

2.5.2.1. Asynchronous receive

The number of bits per character is controlled by the command-code register
W11. Five, seven or eight bits per character may be selected also by this
register. Data is right-justified (to the least significant bits) with the
unused bits set to 1's. The parity of the transmitted character, and the
parity check of a received character can be set to Even, Odd, Mark, Space
and None. The parity bit is transferred to the receive FIFO with the data
if the character length selected, including parity, is 8 bits or less and
can be read out of register R27.

The receiver always checks for a stop bit. If after character assembly the
stop is found to be '0', the framing error bit is set. This error bit is
coupled to the data and can be read in register R27 before the data is read
out.

The Break condition is continuous 0's, as opposed to the usual continuous
ones during idle. The EDRA recognizes the Break condition upon seeing a null
character plus a framing error (see register R27). Upon recognizing this
sequence the break bit will be set (register R27) and will remain set until
a one is received. At this point the Break condition is no longer present.
At the termination of a break the receive data FIFO contains a single null
character which should be read and discarded. The Framing Error bit nor the
Parity Error bit will be set for this character.

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2.5.2.2. Receive interrupts

The receive interrupts of the UART are enabled/disabled as a group by the
Receive Interrupt Enable bit (register W4 RxGIE). If the interrupt
capabilities are not needed, polling may be used. This is selected by
disabling the receiver interrupts and polling the receiver status register
(register R27). If receiver status is to be checked, it must be done before
the data is read because reading the data pops both the data and error
conditions belonging to that data.

The Group Interrupt Pending bit will always be set if one of the receiver
activity detectors are set, but an interrupt will only be given if the
source is enabled and the RxGIE is set.

2.5.2.3. Asynchronous transmit

The number of stopbits that will be transmitted can be selected in
command-code register W11. The setting of character length and parity are
common to both the receiver and the transmitter. In all cases the data is
in the least significant bits of the data word written by the processor.

The transmitter may be programmed to send a Break. To do this the Send
Break bit (register W10) may be written by the processor. Setting of this
bit causes the transmitter to transmit continuous 0's from the first
transmit clock edge after the bit is set, until the first clock edge after
this bit is reset. When this bit is set, the character that's currently
beeing sent shall be corrupted and internally the Tx-FIFO is stopped to
prevent lost of more characters. An additional status bit for use in
asynchronous mode is the All Sent bit. This bit is set when the transmit
shift register is empty and all previous data or stop bits have been shifted
out. This bit can be used by the processor as an indication that the
transmitter may be safely disabled.

2.5.2.4. Transmit interrupts

Transmit interrupts are controlled by the Transmit Group Interrupt Enable
bit. There are a number of transmit interrupt sources: Tx-buffer empty,
Tx-shift register all sent, overflow and, when enabled, the threshold
interrupts.

If the interrupt capabilities are not required polling may be used. This is
selected by a reset of the register W04 TxGIE bit and polling the Tx status
and activity bits in register R20.

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2.5.3. Flow control

The flow control function is used in transmission mode 1C of the EDRA.

Flow control allows the connection of two EDRAs with asynchronous terminals operating at different user data rates, by reducing the character output of the faster to that of the slower terminal. Each EDRA has a data rate setting that is equal to the data rate of the DTE that it is connected to. Between the two EDRA/DTE combinations a rate difference may be present.

Data rate differences between the two EDRAs is taken care of by the end to end flowcontrol mechanism (manipulation of the X-bit in the data stream on the synchronous data interface). While the data transfer between EDRA and DTE is handled with local flow control. This local flow control can be performed by X-ON/X-OFF or by control of lead 106.

According to ECMA, the intermediate rate between the two EDRAs is determined by the calling EDRA. And so two situations be distinguished:

- A fast EDRA/DTE combination calls a slow EDRA/DTE combination;
- A slow EDRA/DTE combination calls a fast EDRA/DTE combination.

These two situations are illustrated in figure 2.5.3-1.

```
calling                                    called
DTE/EDRA (fast)   intermediate rate   DTE/EDRA (slow)

 ┌──────┬──────┐                        ┌──────┬──────┐
 │ DTE  │      │────────────────▷       │      │ DTE  │
 │ 9600 │ EDRA │                        │ EDRA │ 4800 │
 │ baud │      │◁────────────────       │      │ baud │
 └──────┴──────┘                        └──────┴──────┘


calling                                    called
DTE/EDRA (slow)   intermediate rate   DTE/EDRA (fast)

 ┌──────┬──────┐                        ┌──────┬──────┐
 │ DTE  │      │────────────────▷       │      │ DTE  │
 │ 4800 │ EDRA │                        │ EDRA │ 9600 │
 │ baud │      │◁────────────────       │      │ baud │
 └──────┴──────┘                        └──────┴──────┘
```
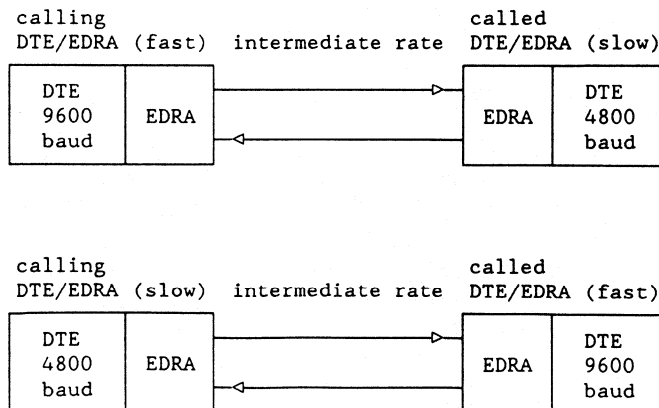
2.5.3-1 Examples of the two flow-control situations.

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When a faster EDRA/DTE calls a slower EDRA/DTE, the situation is illustrated
in figure 2.5.3-2:
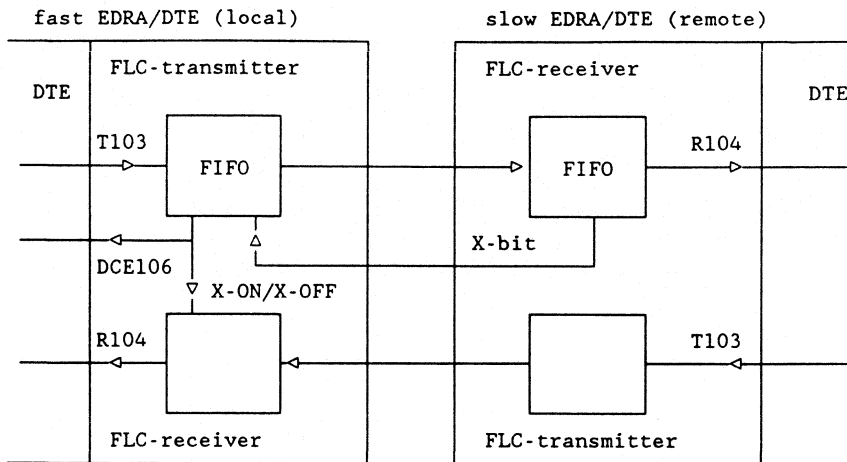
Figure 2.5.3-2 Fast EDRA/DTE calls a slow EDRA/DTE.

In the FLC-receiver of the EDRA at the remote side, data on the synchronous
data interface is coming in faster than it is going out to the DTE. The
FIFO gets filled. When threshold level 1 is reached (see section 2.5.3.1)
the X-bit is turned off ('1'). When the FLC-receiver of the local EDRA
detects the X-bit to be turned off, transmission of data over the
synchronous data interface is blocked. While data is still coming from the
local DTE, the data in the FIFO at the local EDRA reaches the threshold
level 1. (This threshold level is also reached is the local DTE transmits
with overspeed.) At this point an interrupt (EDRA transmitter TH1) is
generated (if enabled). When the command 'AUTO 106' has been given, the DTE
will be stopped with lead DCE106. If the connected DTE can only handle
XON/XOFF, also 'AUTO XON/XOFF' can be selected. After the local DTE has
stopped transmitting data, and the remote EDRAs FIFO level has decreased
below threshold level 2, the X-bit will be turned on. The FIFO level from
the local EDRA will decrease and lead DCE106 becomes high or a X-ON
character will be generated by the EDRA.

The remote control with the X-bit is called end-to-end flow control. The
situation at the calling DTE/EDRA, caused by the end-to-end flow control and
the overspeed of the DTE, is handled as local flow control.

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The second situation the calling DTE/EDRA (local) is slower as the called
DTE/EDRA (remote). This situation is illustrated in figure 2.5.3-3.
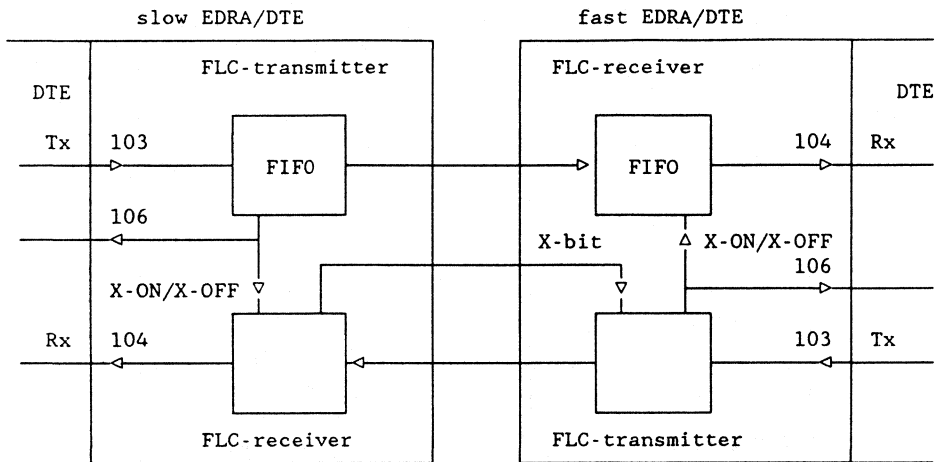
Figure 2.5.3-3 Slow EDRA/DTE calls fast EDRA/DTE.

At the local side, the DTE can cause overspeed due to the fact that the
intermediate is determined by the local EDRA. This overspeed is handled with
local flow control.

The remote DTE transmits its data faster than the synchronous data interface
can handle. Also this situation is solved with the local flow control
procedure.

The X-bit in the data stream from local to remote DTE/EDRA is still used,
but is continu ON ('0'), unless overspeed occurs because of insertion
X-ON/X-OFF characters in the receiver at the local side.

2.5.3.1. Flow control FIFOs

The FIFOs, which are used for flow control, have a capacity of 32 bytes.
They are equiped with two threshold level detectors, which can be programmed
in registers W12 and W14 (section 2.9.1). The threshold detectors give an
indication if the contents of the FIFO is higher than level 1 or lower than
level 2. An illustration of the FIFOs is given in figure 2.5.3.1-1.

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```
                          | DATA IN
             FIFO         ▽
                          |
           ┌──────────────┬─────────┐
           │              │     TOP │
           │              │
           │·············│───── THRESHOLD 1 (X-OFF)
           │              │
           │              │
           │              │
           │·············│───── Threshold 2 (X-ON)
           │              │
           └──────────────┴─────────┘
                          │  BOTTOM
                          |
                          ▽
                          | DATA OUT
```
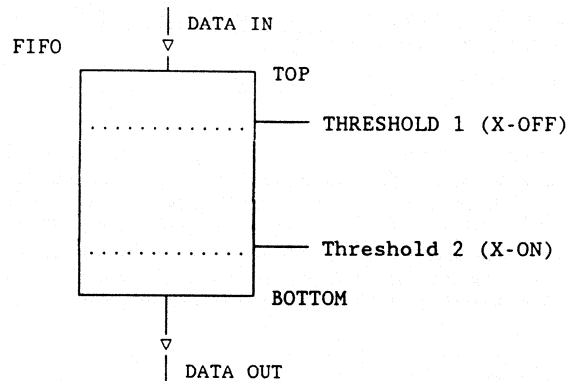
Figure 2.5.3.1-1. Flow control FIFO.

For both receiver- and transmitter FIFO a threshold register is available to
be able to program both threshold levels. The register is divided into two
parts. The first part contains threshold level TH1 (4 bits), the second part
contains threshold level TH2 (4 bits) (see section 2.9.1.13). Both
thresholds can only have an odd values. With the four bits in the threshold
register only the four most significant bits can be programmed. The least
significant bit is always 1. So all odd threshold levels between 1 and 31
can be programmed.

2.5.3.2. FIFO threshold levels

The setting of the FIFO threshold levels concerning flow-control, depends on
the type of data connection. Determining factors are whether the EDRA is on
the calling or called side of a data connection, and if its DTE data rate is
faster or slower than the data rate of the DTE at the remote EDRA.

Resuming, there are 4 different situations:

1. The EDRA is at the calling side of the connection, local DTE is faster
than remote.
2. The EDRA is at the calling side of the connection, local DTE is slower
than remote.
3. The EDRA is at the called side of the connection, local DTE is slower
than remote.
4. The EDRA is at the called side of the connection, local DTE is faster
than remote.

Each situation requires it specific setting of the threshold levels of the
FIFOs. The settings are determined by the following characteristics:

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-Overspeed of the DTE;
-DTE responce on lead 106 or X-OFF, the number of characters transmitted by
the DTE after "X-OFF" or DCE106 LOW;

-Local/remote DTE data rate difference;
-Delay of the network.

Flow control can be used in different ways, automatically or microprocessor
controlled. The flowcontrol mode can be set in write register W00 (section
2.9.1.1). The specific flowcontrol features can be selected in write
register W11 (section 2.9.1.12). The monitoring of flowcontrol is performed
by the FIFO threshold levels 1 and 2. When threshold level TH1 is reached,
the incoming data must be stopped as soon as possible. When the level drops
below threshold level TH2, the FIFO can accept data again.

2.5.3.3. <u>End to end flowcontrol</u>

For end to end flowcontrol, the X-bit in the synchronous data interface
frame controls the transfer of data via that interface. The end to end flow
control can be automatically performed by the EDRA or can be managed by the
microcontroller.

If the EDRA is in the automatic flow control mode the X-bit is switched ON
and OFF according the values of the threshold levels TH1 and TH2 of the FLC-
receiver. In figure 2.5.3.3-1 the switching of the X-bit is illustrated.

```
                                                    set X-bit OFF
                                                         △
                                                         |
   ┌──────────┐       ┌──────────┐       ┌──────────┐
   │ TH1 = 0  │◄──────│ TH1 = 0  │◄──────│ TH1 = 1  │
   │ TH2 = 0  │──────►│ TH2 = 1  │──────►│ TH2 = 1  │
   └──────────┘       └──────────┘       └──────────┘
        |
        ▽
  set X-bit ON
```
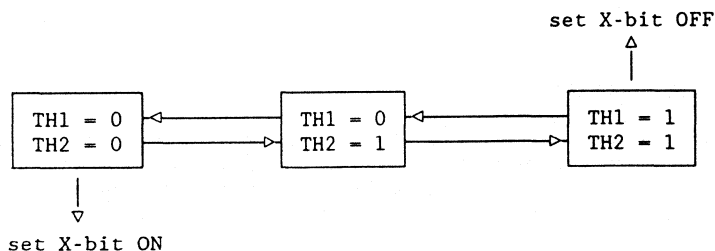
       Figure 2.5.3.3-1 X-bit control by the threshold levels.

When the EDRA is not in automatic mode, the microcontroller must know the
state of the FIFO thresholds of the FLC-receiver to be able to perform
flowcontrol.

The threshold levels can be monitored by polling read register R20 (section
2.9.2.1) or if bit THD GIE of write register W04 is enabled and (TH1=0 and
TH2=0) or (TH1=1 and TH2=1) an interrupt will be generated.

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The microcontroller has to perform the following actions:

If an interrupt was generated and the interrupt source was the FLC-receiver
TH1 or (in polling mode) TH1 = 0, the X-bit must be clamped '1' (OFF)

In an interrupt was generated and the interrupt source was the FLC-receiver
TH2 or (in polling mode) TH2 = 1, the X-bit must be clamped '0' (ON)

The remote EDRA will stop the transmission of data on the synchronous data
interface when the received X-bit is ON. When the received X-bit is OFF, it
can restart transmission.

2.5.3.4. Local flowcontrol

If local flow control is performed in automatic mode the EDRA performs the
folling actions:

When threshold level TH1 is reached at the FLC transmitter, the transmission
of data from DTE to the EDRA must be stopped. If the FIFO level of the FLC
transmitter drops below threshold level TH2, the DTE can start the data
transmission again.

The EDRA can start and stop the transmission of the DTE data in two ways:

-In the 'AUTO 106' mode lead DCE106 will be controlled by the flow control
logic.
-If the EDRA is in 'AUTO XON/XOFF' mode, character 'X-OFF' (DC3 ASCII) or
'X-ON' (DC1 ASCII) are inserted in the data, and transmitted via lead T104
to the DTE. The ASCII code for XON/XOFF can be downloaded in write registers
W16 and W17).

If the local flowcontrol is performed by the microcontroller, the threshold
levels TH1 and TH2 can be monitored by polling read register R20 (section
2.9.2.1) or if bit THD GIE of write register W04 is enabled and (TH1=0 and
TH2=0) or (TH1=1 and TH2=1) an interrupt will be generated. The actions that
must performed on the interrupt from TH1 and TH2 of the URF-transmitter are
illustrated in figure 2.5.3.4-1.

interrupt- source	DTE reacts on lead DCE106	DTE reacts on XON/XOFF character
TH1 = 1	clamp DCE106 to 1 (OFF)	EDRA sends one X-OFF character
TH2 = 0	clamp DCE106 to 0 (ON)	EDRA sends one X-ON character

Figure 2.5.3.4-1 Local flowcontrol procedure by μC.

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2.5.3.5. <u>X-ON/X-OFF</u>

The X-ON and X-OFF characters can be downloaded by the microcontroller into register W16 and W17 (section 2.9.1). Only the data must be written, parity, start and stop bits will be auto generated by the EDRA according the settings in register W11 (section 2.9.1.12).

The X-ON/X-OFF characters are generated by the EDRA in the AUTO X-ON/X-OFF mode. However the X-ON/X-OFF characters can be inserted in the data stream on lead T104 by microcontroller (see register W11).

It is possible to filter the X-ON/X-OFF characters that are received on lead T103. This can only be done if they do not contain any parity and/or frame errors. This feature is needed when local flow-control is used with X-ON/X-OFF because if a X-ON/X-OFF character is transmitted to the remote EDRA/DTE, the local flow-control at this remote EDRA/DTE can be disturbed. These filter can prevent the transfer of X-ON/X-OFF characters in the data stream to the remote EDRA. The filters can be enabled/disabled by μC in write register W11.

The default setting of the filters (when a transmission mode is selected in write register W00) is 'OFF' (no filtering). When in transmission mode 1C (flow-control) the AUTO X-ON/X-OFF mode will be selected, both filters will be active.

Two data switches are implemented in URF. One in the data path from T103 to SDO (just after the Rx-FIFO), and one in the data-flow from SDI to R104 (just after the Tx-FIFO). By switching the data switches the data flow inbvolved can be stopped.

Both switches can be independently enabled/disabled by the microcontroller, or be controlled by the X-bit from SDI for the Rx data switch and controlled by the X-ON/X-OFF character-detection (T103) for the Tx data switch.

The settings for control of the data switches are written in register W11 by microcontroller.

By selection of any transmission mode, both the Tx and Rx data switches will be enabled, except for transmission mode 1C. In this case the data switches will be controlled by the X-bit from the remote EDRA. When in transmission mode 1C 'AUTO X-ON/X-OFF' mode is selected, the Tx data switch will be default controlled by the X-ON/X-OFF character recognition.

In figure 2.5.3.5-1 the data paths of the EDRA in flowcontrol mode are illustrated.

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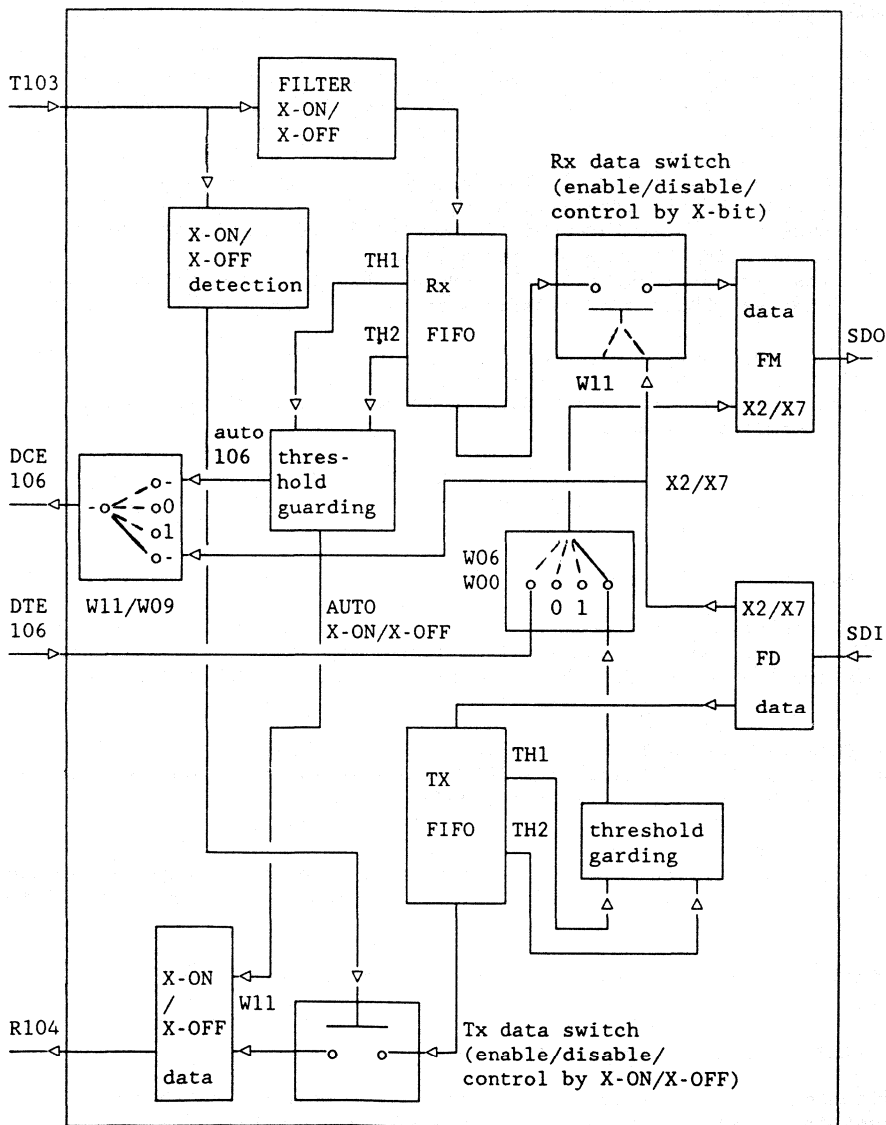
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Figure 2.5.3.5-1 Flow control in the EDRA.

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2.6. Inband Parameter Exchange

The EDRA allows transfer of parameter information within the user data
stream of an established connection. This transfer of parameter information
is called Inband Parameter Exchange (IPE). The EDRA supports the three
different types of IPE that are recommended by ECMA-102:

- asynchronous IPE mode with RA0 coded data in the 64 kbit/s
  channel (EDRAs transmission mode 3B).
- unrestricted synchronous IPE mode at 64kbit/s rate in the 64 kbit/s
  channel (EDRAs transmission mode 3C).
- restricted synchronous IPE mode at 56kbit/s rate in the 64 kbit/s
  channel (EDRAs transmission mode 3C).

and also is supported:

- multiple sampling coded data in the 64 kbit/s channel (EDRAs
  transmission mode 3A).

In all four modes the transmit data is to be written into write register
W15 while the received data must be read from read register R26.

2.6.1. Asynchronous IPE mode

In the asynchronous IPE mode, the data is RA0 coded on an intermediate rate
or 64 kbit/s channel. The number of data bits in a data byte, the number of
stopbits and the parity bit should be programmed in the UART (see section
2.5.2).

In the ECMA recommendations IPE is specified for three speeds: 19200, 9600
and 4800 bit/s. The EDRA supports IPE for all RA0 speeds. The interchange
circuits can be used as in all other modes.

Data written to register W15 and is placed in the Tx-FIFO. Then it is
shifted out on the synchronous data interface. When all data is transmitted,
the transmitter starts sending 1's until a new character is available for
transmission.

The received data can be readout of the Rx-FIFO (read register R26).

2.6.2. Synchronous IPE mode at 64 kbit/s

The synchronous IPE function for unrestricted transfer. For this mode only
one additional setting must be done in write register W11: the character
length should be set on 8 bits/char. Data written to register W15, will be
placed in the Tx-FIFO and is shifted out on the synchronous data interface,
without additions. When the Tx-FIFO is empty, the last byte that was
transmitted, will be repeated until a new character is available.

The received data can be readout of the Rx-FIFO (read register R26).

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2.6.3. Restricted synchronous IPE mode at 56 kbit/s

The synchronous IPE function for restricted transfer. For the EDRA this mode is equal to unrestricted 64 kbit/s IPE mode.
For this mode only one additional setting must be done in write register W11: the character length should be set on 8 bits/char. Only the lowest 7 bits can be used in write register W15. The MSB should be set '1'. The data written to register W15, will be placed in the Tx-FIFO and is shifted out on the synchronous data interface, without additions. When the Tx-FIFO is empty, the last byte that was transmitted, will be repeated until a new character is available.

The received data can be readout of the Rx-FIFO (read register R26).

2.6.4. Multiple sampling IPE mode

In the multiple sampling IPE mode, the data is coded according the multiple sampling method and placed in the 64 kbit/s channel. The number of data bits in a data byte, the number of stopbits and the parity bit should be programmed in the UART (see section 2.5.2).

The data that is written in register W15, will be placed in the Tx-FIFO and is shifted out to the multiple sampling coder. When all data is transmitted, the transmitter starts sending 1's until a new character is available for transmission.

The received data can be readout of the Rx-FIFO (read register R26).

2.7. Network independent clocking

When the EDRA must adapt synchronous data of which the timing is not synchronised to the EDRA timing, a method, called bit-stuffing is used to enable transfer of those data signals (for V-series only). The EDRA supports the NIC function as it is decribed in the ECMA-102/CCITT V.110 recommendations.

In this section the term modem-clock (on lead S113) will be used when the independent clock is meant and EDRA-clock (on lead S114) for the system locked clock.

The NIC function consists of the following parts:

- a phase comparator that measures the phase difference between the EDRA- and modem-timing and a buffer for transmit data.
- a coder that provides the E-bits in the synchronous data interface bitstream with compensation information.
- and a decoder to translate the incoming E-bits of the synchronous data interface to data and clock correction.

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In figure 2.7-1 a blockdiagam is illustrated of the NIC transmitter while in figure 2.7-2 the NIC receiver is illustrated.
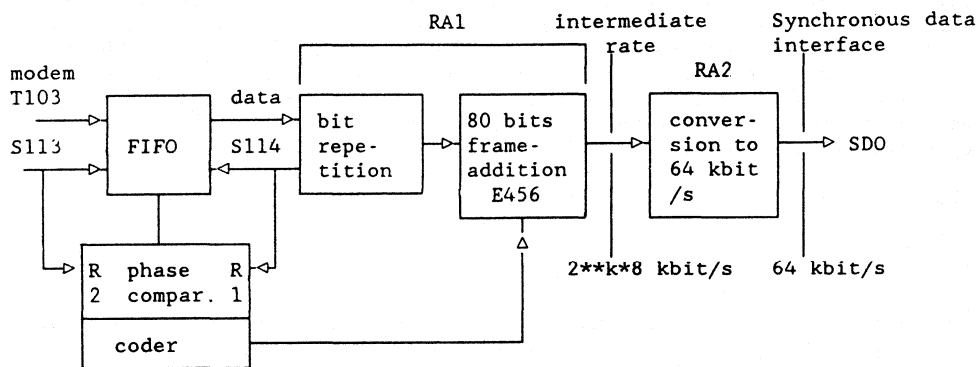
Figure 2.7-1 Block diagram of the NIC transmitter.
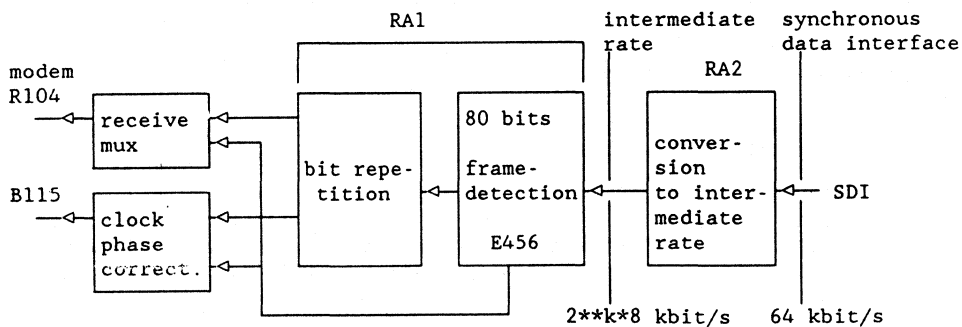
Figure 2.7.2 Block diagram of the receiver.

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2.7.1. <u>NIC transmitter</u>

The measurement of the phase difference:

The phase difference between the following two frequencies is measured
(according to ECMA-102 recommendation):

R1 = 0.6 * intermediate rate of the EDRA (synchronised to EDRA)
R2 = 0.6 * intermediate rate of the modem, derived from and synchronised to
the modem signal element timing

The relation between R1, R2 and their intermediate rate is depicted in table
2.7.1-1.

intermediate rate	R1,R2
8000	4800
16000	9600
32000	19200

Table 2.7.1-1 Nominal R1/R2 frequencies for given intermediate.

Phase measurements are given relative to R1 by the formula below:

PD (phase difference) = phase(R2) - phase(R1)

The system will know the next five phases: 0%, 20%, 40%, -40%, -20%. These
phases will be coded and transmitted to the receiving EDRA in the E-field
(of the 10 bytes frame).

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Compensation:

The next drawing shows the states of the phase of R2 relative to R1.
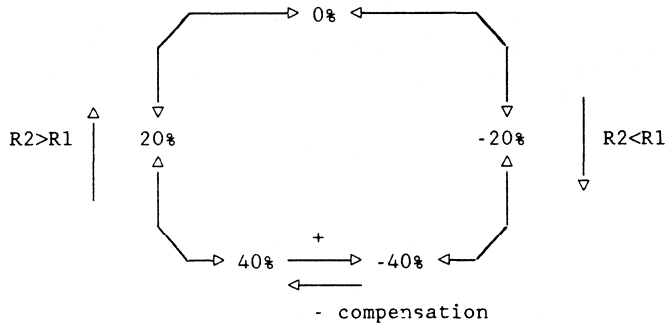
Figure 2.7.1-2 Network independent clocking state diagram.

Every 10 bytes frame the EDRA connected to the modem codes the phase difference state into the E4, E5 and E6 positions of the E-field. To avoid continuous jitter in the transmitted code, it will be changed after an increased phase difference of 15% (of the R1 clock period). So, a code 000 (20%) will be changed in 001 (40%), when the measured phase difference is 35% or more, and changed in 111 (0%) when 5% or less.

In the case the data rate of the modem is higher than the rate of the EDRA the situation occurs that the phase difference is 40%. When the phase difference is 40%, the modem nearly transmits more information than the EDRA can handle. At a certain moment the phase difference will be 55%. This means that the EDRA will miss one data bit received from the modem. With the compensation method this bit will be transmitted in the E-bits. This is called positive stuffing and the transmitted code will indicate compensation of a binary 1 or 0.

In the case the data rate of the modem is lower than the rate of the EDRA the situation occurs that the phase difference is -40%. When the phase difference is -40%, the EDRA is nearly transmitting more information than the modem offers. At -40% to 40% transition the code indicates the receiving EDRA to 'stuff' a bit (negative compensation). In table 2.7.1-3 the coding of the E-bits used for network independent clocking is illustrated.

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Displacement (in % of nominal R1 clock period at n * 4800 bps, n=1, 2 or 4)	Coding in the 80-bits frame		
	E4	E5	E6
nominally 0	1	1	1
+20	0	0	0
+40	0	0	1
-40	0	1	0
-20	0	1	1
Compensation control	E4	E5	E6
Positive compensation of binary 1	1	0	1
Positive compensation of binary 0	1	0	0
Negative compensation	1	1	0

Table 2.7.1-3 Coding of the E bits.

2.7.2. <u>NIC receiver</u>

The NIC receiver contains a decoder/phase shifter and a receiver data-mux.
By means of the received frame, the phase of the receiver-clock (to DTE)
must be changed in steps of 20%, as described in chapter 2.7.1.
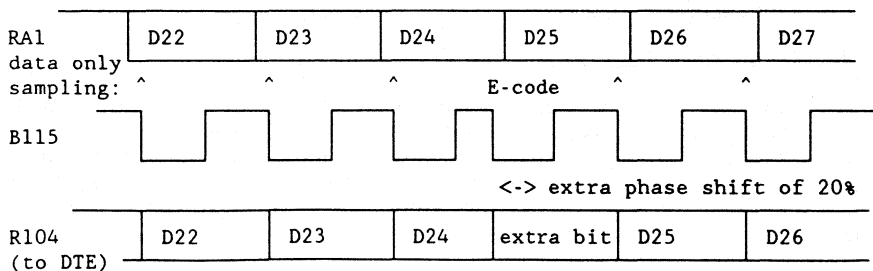
Figure 2.7.2-1 Positive compensation.

Figure 2.7.2-1 shows the received data (from the RA1) and the EDRA clock.
In the previous frames the E4, E5 and E6 bits indicated a phase shift that
resulted in a +40% clock. After bit D24 a new E-Field is received indicating
positive-compensating of a bit. This results in new phase shift of the clock
of 20% to +60% (-40%).The received data-mux now selects the extra bit coming
from the E-Field. The next clock-edge will be just in time to sample bit
D25. The achieved clock-delay will now be -40%.

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| RA1 | D23 | D24 | D25 | D26 | D27 | D28 |

sampling:

B115

<-> extra phase shift of +20%

| R104 (to DTE) | D22 | D23 | D24 | D26 | D27 | |
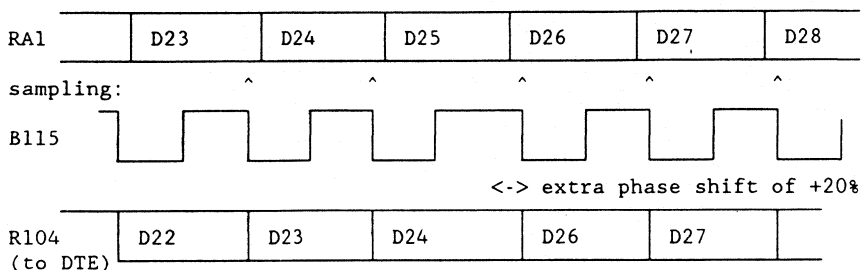
Figure 2.7.2-2 Negative compensation.

Figure 2.7.2-2 shows a -40% clock. The next received E-field indicate a negative compensation. This will result in an extra clock-delay of 20% to -60% (+40%). After this clock shift, bit D25 will be skipped.

The place in the framing where compensation takes place is bit D25. Positive compensation inserts a bit between D24 and D25, negative compensation deletes bit D25.

Max frequency deviation modem clock for 4800, 9600 and 19200 bit/s = +/- 0.347 % while the allowed jitter on modem clock for 4800, 9600 and 19200 bit/s is 1 bit jitter on 48 bits interval. This is a 1.97 % modem clock deviation, provided that the mean deviation over 48 bits is zero.

2.8. Frame mapping/demapping and multiple sampling

2.8.1. Multiple sampling method

For asynchonous user data to synchronous 64 kbit/s conversion, the EDRA has the multiple sampling method available as it is implemented in its predecessor the PCB2320 DRA. Every asynchronous data rate lower than or equal to 19200 bit/s can be adapted without a specific speed setting on the EDRA (the local and remote DTE however should have the same data rate setting).

Concerning the interchange circuits, two points must be taken into account: The EDRA must be in X30-mode (see register W00, section 2.9.1.1). The relation between ON/OFF of the interchange circuits and the binary values of the S- and X-bits on the synchronous data interface should be according the ECMA-102 september definition (see section 2.3.2).

This coding/sampling method is based on the technique of multiple sampling with additional transition coding as depicted in CCITT recommendation R.111.

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This method doesn't recognise character lenght or start-stop bits. It samples the incoming data with 96 kHz. Only transitions are coded in two bits: a transition bit T and coding bit C.

The transition bit T is used to indicate the polarity after a transition, and the second bit C (coding) defines in which half A or B of a 48 kbit/s clock period the transition has occurred. Transitions of data rates upto 24 kbit/s can be coded by the 48 kbit/s. Because one bit can discriminate two phases (A or B), the sampling frequency has to be 96 kHz.

In the lower data-rates, more than two 48 kHz pulses will fall between two signal element transitions. In this case the resulting 48 kbit databits P (polarity) will repeat the polarity and are therefore equal to the previous bit T.

The phase jitter on the received data stream varies for the different bit rates from 20 % for 19.2 kbit/s down to 2.5 % for 2400 bit/s or even lower for slow data.

The 48 kbit/s data stream is further handled as 48 kbit/s synchronous data stream.

In appendix C the multiple sampling method is illustrated.

2.8.2. Frame mapping/demapping

For synchronous data rates of 600, 1200, 2400, 4800, 9600, 19200 and 38400 bit/s, a X.30/V.110 defined multiframe of 10 bytes bits is used (see appendix B). It consists of two 5 bytes frames, using subrates of 8, 16 and 32 kHz. An incoming data rate will be first translated to the next higher rate expressed by $2**k * 8$ kHz where k=[0,1,2,3] (see table 2.8.2-1). For speeds 600, 1200, 2400 a first rate adaption to 4800 bit/s is done by bit repetition. This first stage of rate adaption is called the RA1 function and is illustrated in figure 2.8.2-2.

Data rate (bit/s)	framespeed (Hz)
600, 1200, 2400, 4800	8000
9600	16000
19200	32000
38400	64000

Table 2.8.2-1 First step in data rate adaption.

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```
                    synchr. user              intermediate  synchronous
   asynchr.         data 600-                 rate          data interface
   user      RA0    38400 bit/s    RA1                       RA2
   data
              ┌──────────┐          ┌──────────┐ ┌──────────┐  ┌──────────┐
              │ asyn./   │          │          │ │ 80 bits  │  │          │
   ───────────│ synchron.│──────────│bit repe- │─│ frame-   │──│ convers. │───────
              │ conversion│         │ tition   │ │ addition │  │ to 64 k  │
              └──────────┘          └──────────┘ └──────────┘  └──────────┘

   <=19.2 kbit/s   2**n*600 bit/s              2**k*8 kbit/s    64 kbit/s
```
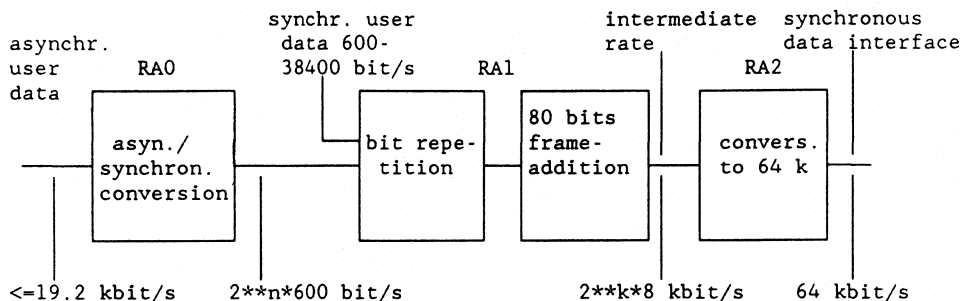
Figure 2.8.2-2 Bit rate adaption of synchronous data received from the RA0
blocks and synchronous user data <=38400 bit/s.

The multiframe consists of 10 bytes containing 8*6 data bits, 8 S-bits, two
X-bits, 17 bits for the frame synchronisation pattern and 7 E-bits used for
the following purposes:

E1	E2	E3	E4	E5	E6	E7
speed indication for remote EDRA			network independ. clocking code-bits			600 and 1200 bit/s multiframe syncbits

The three speed indication bits can be filled in via the μC-interface and
are transmitted to the remote EDRA transparently. The E4 to E6 bits are used
to transmit the positive or negative bit-stuffing coding. Bit E7 is used for
slow-data synchronisation purposes (see section 2.9.1.4).

The data rate conversion is completed after the conversion of the
intermediate rate to 64 kbit/s by block RA2 as illustrated in figure 2.8.2-
2.

The 48, 56 and 64 kbit/s synchronous user data are adapted to 64 kbit/s in
one step using a 32 bit frame. Asynchronous user data $\leq$ 19200 bit/s, that is
coded with the multiple sampling method, is also inserted at this level as a
48000 bit/s data stream. In figure 2.8.2-3 this rate adaption stage is
illustrated.

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synchronous user data
48, 56 and 64 kbit/s

asynchronous
user data

FM (contains RA1/2 functions)

```
        ┌─────────────┐        ┌──────────┐
        │ multiple-   │        │          │    synchronous data
        │ sampling    │        │ 32 bit   │    interface
────────│ asynchr./   │────────│ framing  │───────────────
        │ synchr.     │        │ set-up   │
        │ convertor   │        │          │
        └─────────────┘        └──────────┘
```

<=19.2 kbit/s   48 kbit/s   64 kbit/s
                     synchronous data
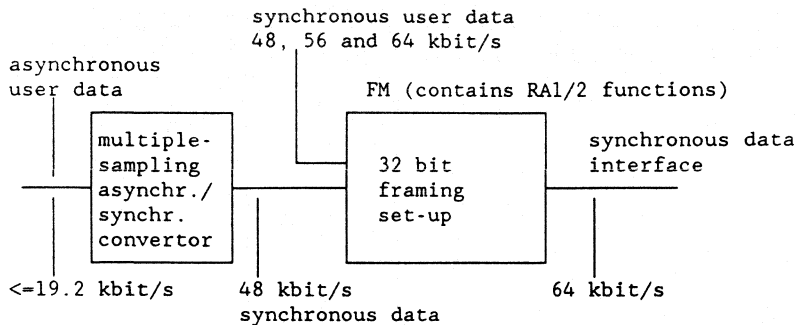
Figure 2.8.2-3 Bit rate adaption of synchronous user data >=48000 bps and
asynchronous user data (multiple sampling).

For the data rate of 48000 bit/s a 32 bits frame is used (see appendix B).
This frame consists of 4 bytes containing 4*6 data bits, 3 S-bits, one X-
bit and 4 frame synchronisation bits.

For the data rate of 56000 bit/s the 32 bits frame structure is used (see
appendix B). Only now 4*7 bits consist for data and four S-bits. No frame
bits for synchronisation can be used.

For the data rate of 64000 bit/s no rate adaption is needed and the DRA is
transparent for this speed (see appendix B).

2.9. Microcontroller interface

The EDRA is controllable by the 8-bit INTEL compatible microcontroller bus.

The bus consists of:

* 8 data/address multiplexed I/O lines (DB7 to DB0)
* A read not input (RDN)
* A write not input (WRN)
* An address latch enable input (ALE)
* A chip select not input (CSN)
* An interrupt not open drain output (INTN)

When ALE is HIGH and the EDRA is selected, the address on the DB7-DB0 I/O
port is latched into the address latch. One of the eightteen write registers
or one of the nine read registers may be selected (see table 2.9-1). This
selection is made by the five least significant data/address lines (DB0-DB4)
and the CSN signal whereby the EDRA is selected by CSN and register is
selected by the address lines.

When RDN is LOW the EDRA writes the data byte from the selected read
register to the data-bus I/O port. On the leading edge of WRN, the data-byte
from the data-bus I/O port is written into the addressed write register.

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DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	address	write reg	read reg
X	X	X	0	0	0	0	0	0	W0	-
X	X	X	0	0	0	0	1	1	W1	-
X	X	X	0	0	0	1	0	2	W2	-
X	X	X	0	0	0	1	1	3	W3	-
X	X	X	0	0	1	0	0	4	W4	-
X	X	X	0	0	1	0	1	5	W5	-
X	X	X	0	0	1	1	0	6	W6	-
X	X	X	0	0	1	1	1	7	W7	-
X	X	X	0	1	0	0	0	8	W8	-
X	X	X	0	1	0	0	1	9	W9	-
X	X	X	0	1	0	1	0	10	W10	-
X	X	X	0	1	0	1	1	11	W11	-
X	X	X	0	1	1	0	0	12	W12	-
X	X	X	0	1	1	0	1	13	W13	-
X	X	X	0	1	1	1	0	14	W14	-
X	X	X	0	1	1	1	1	15	W15	-
X	X	X	1	0	0	0	0	16	W16	-
X	X	X	1	0	0	1	0	17	W17	-
X	X	X	1	0	1	0	0	20	-	R20
X	X	X	1	0	1	0	1	21	-	R21
X	X	X	1	0	1	1	0	22	-	R22
X	X	X	1	0	1	1	1	23	-	R23
X	X	X	1	1	0	0	0	24	-	R24
X	X	X	1	1	0	0	1	25	-	R25
X	X	X	1	1	0	1	0	26	-	R26
X	X	X	1	1	0	1	1	27	-	R27
X	X	X	1	1	1	0	0	28	-	R28

Table 2.9-1 Register addresses.

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2.9.1. Registers W0-W17

In this section the bit assignment of the write registers is illustrated.

EDRA-mode control:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W0	-	-	FSINV	TRM2	TRM1	TRM0	ICM1	ICM0
W1	V7	V6	V5	V4	V3	V2	V1	V0
W2	LLP1	LLPCI	LLP3	RLP4	RLP2	E3	E2	E1
W3	SDO−1	SG2	SG1	SG0	FM1	FM0	E7	NoCCITT

Table 2.9.1-1 Bit assignment;register W0, W1, W2, W3.

General interrupt control:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W4	MIE	-	-	ICGIE	THGIE	OOSIE	TxGIE	RxGIE

Table 2.9.1-2 Bit assignment;register W4.

Input interchange circuits:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W5	R104IE	T103IE	C105IE	V108IE	MI2IE	MI1IE	DTE106 IE	SXI
W6	T103−1	T103−0	C105−1	C105−0	V108−1	V108−0	DTE106 −1	DTE106 −0
W7	S9	S8	X7	S6	S4	S3	X2	S1

Table 2.9.1-3 Bit assignment;register W5, W6, W7.

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Output interchange circuits:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W8	S9IE	S8IE	X7IE	S6IE	S4IE	S3IE	X2IE	S1IE
W9	R104-1	R104-0	DCE106 -1	DCE106 -0	107-1	107-0	I109-1	I109-0
W10	TXsebr	MO1	B115=1	S114=1	-	MO2	-	SXO

Table 2.9.1-4 Bit assignment;register W8, W9, W10.

Selections for URF (UART/RA0/Flowcontrol):

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W11	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Table 2.9.1-5 Bit assignment;register W11.

URF receiver FIFO thresholds:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W12	TH2A4	TH2A3	TH2A2	TH2A1	TH1A4	TH1A3	TH1A2	TH1A1

Table 2.9.1-6 Bit assignment;register W12.

URF mode bits:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W13	RxFrEr IE	RxPar IE	RxBreak IE	Rx/TxOf IE	RxChAv IE	TxFIFOe IE	TxAllSe IE	XonXoff IE

Table 2.9.1-7 Bit assignment;register W13.

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URF transmitter FIFO thresholds:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W14	TH2A4	TH2A3	TH2A2	TH2A1	TH1A4	TH1A3	TH1A2	TH1A1

Table 2.9.1-8 Bit assignment;register W14.

UART Transmit buffer:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W15	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

Table 2.9.1-9 Bit assignment;register W15.

(Flow control) XON/XOFF code:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W16	XON 7	XON 6	XON 5	XON 4	XON 3	XON 2	XON 1	XON 0
W17	XOFF 7	XOFF 6	XOFF 5	XOFF 4	XOFF 3	XOFF 2	XOFF 1	XOFF 0

Table 2.9.1-10 Bit assignment;register W16, W17.

2.9.1.1. Register W00

Bit ICM0 and ICM1: Bit ICM0 and bit ICM1 are used to select the mode of the interchange circuits as the are described in section 2.3. The modes are illustrated in table 2.9.1.1-1.

IC0	IC1	mode
0	0	V.110
0	1	μC
1	0	X.30
1	1	not used

Table 2.9.1.1-1. interchange circuit modes.

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Bit TRM0 to TRM2: Bit TRM0 to TRM2 are used to select the transmission mode
of the EDRA. The transmission modes of the EDRA are described in section
2.2. The relation between bits TRM0 to TRM2 and the transmission mode of the
EDRA are depicted in table 2.9.1.1-2.

TR2	TR1	TR0	Transmission mode	
0	0	0	1A synchronous	(DTE-DTE)
0	1	0	1B asynchronous RA0	(DTE-DTE)
0	1	1	1C asynchronous FLC	(DTE-DTE)
0	0	1	1D asynchronous MS	(DTE-DTE)
1	0	0	2 asynchronous	(DTE- μC)
1	1	0	3A asynchronous MS	(μC - 64kbit/s)
1	0	1	3B asyn. RA0 (IPE-RA0)	(μC - 64kbit/s)
1	1	1	3C IPE-64/56kbit/s	(μC - 64kbit/s)

Table 2.9.1.1-2 Transmission mode of the EDRA.

Note 1: when mode 1D (asynchronous multiple sampling) is selected, the speed
selection in W01 must be set to 48 kbit/s.

Note 2: If no flow control is selected (any other mode than mode 1B) the
next actions must be taken to disable the flowcontrol-auto modes:

*For mode 1A: Write to register W11: 24H.
*For mode 1B: Write to register W11: 24H and
                    to register W12: FFH.
*For mode 1C: Write to register W12: 24H.
*For mode 3 : No special actions, interchange interface leads should be
                    clamped.

Bit FSINV: Frame select inversion. When FSINV is set to '0': FSX/R leading
edge triggers frame select. This situation is described in section 2.4 and
illustrated in figure 2.4.1-1. When FSINV is set to '1': FSX/R trailing edge
triggers frame select (the inverse frame select signals can be provided to
the EDRA).

2.9.1.2. Register W01

Bits V0 - V4: bits V0 - V4 determine the synchronous data rate at the
interchange interface for the adaption of synchronous user data. They also
determine the synchronous data rate in which the output data of the RA0
block is placed (in case of RA0 asynchronous user data rate adaption). The
NIC data rates can also be selected by V0 - V4. The settings of V0 - V4 are
illustrated in table 2.9.1.2-1.

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V4	V3	V2	V1	V0	Frame speed	Intermediate	remarks
0	0	0	0	1	600	8000	
0	0	0	1	0	1200	8000	
0	0	0	1	1	2400	8000	
0	0	1	0	0	4800	8000	
0	0	1	0	1	9600	16000	
0	0	1	1	0	19200	32000	
0	0	1	1	1	38400	64000	
0	1	0	0	0	48000 *)	64000	
0	1	0	0	1	56000	64000	
0	1	0	1	0	64000	64000	
0	1	1	0	0	1200/75	8000	Split
0	1	1	0	1	75/1200	8000	speeds
1	0	1	0	0	4800	8000	NIC
1	0	1	0	1	9600	16000	speeds
1	0	1	1	0	19200	32000	

*) In transmission mode 1D, Multiple sampling mode (see register W00), 48000 bps must be selected.

Note: for split speed interchange connections to the DTE see appendix D.

Table 2.9.1.2-1 Synchronous data rate selection.

Bit V5 - V7: bit V5 - V7 determine the asynchronous data rate of the URF receiver/transmitter. These settings are used in transmission mode 1B, 1C, 1D, 2, 3A and 3B. In table 2.9.1.2-2 the settings of V5 - V7 are illustrated.

V7	V6	V5	URF rate (baud)
0	0	0	300
0	0	1	600
0	1	0	1200
0	1	1	2400
1	0	0	4800
1	0	1	9600
1	1	X	19200

Table 2.9.1.2-2 URF rate selection.

Extended data rate adaptor

2.9.1.3. Register W02

Bits E1, E2 and E3: In every 10 bytes multiframe (for user data rates not exceeding 38400 bit/s), E1 to E3 are available to transmit information about the data rate setting to the remote subscriber. The information to be filled in, is illustrated in table 2.9.1.3-1.

data rate (bit/s)	E1	E2	E3
600	1	0	0
1200	0	1	0
2400	1	1	0
4800	0	1	1
9600	0	1	1
19200	0	1	1

Table 2.9.1.3-1 Setting of E1 - E3.

Bit RLP2: If bit RPL2 is made '1' remote test loop 2 is set. In this testloop circuit R104 is inside the EDRA connected to circuit T103 and circuit I109 is inside the EDRA connected to circuit C105. This remote testloop is illustrated in figure 2.9.1.3-2.

Bit RLP4: If bit RLP4 is made '1' remote testloop 4 is set. In this testloop circuit T103 is inside the EDRA connected to circuit R104. The serial data input is inside the EDRA connected to the synchronous data output. The remote testloop 4 is illustrated in figure 2.9.1.3-3.

Bit LLP3: If bit LLP3 is made '1' local testloop 3 is set. In this testloop the synchronous data output is inside the EDRA connected to the synchronous data input. The local testloop 3 is illustrated in figure 2.9.1.3-4.

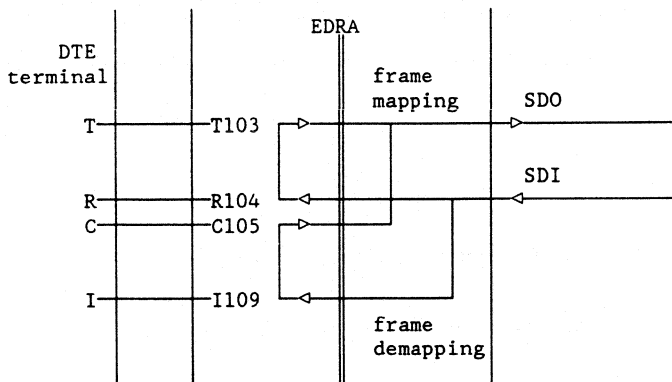# Extended data rate adaptor

Figure 2.9.1.3-2 remote testloop 2
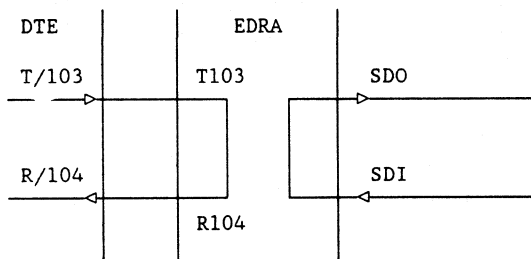
Figure 2.9.1.3-3 remote testloop 4
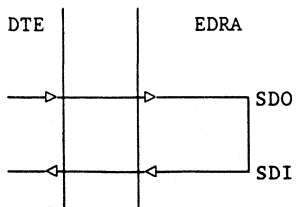
Figure 2.9.1.3-4 local testloop 3

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Bit LLPCI: If bit LLPCI is made '1' local testloop C—▷I is set. In this
testloop the input C105 is inside the EDRA connected to the I109 output. The
local testloop C—▷I is illustrated in figure 2.9.1.3-5.

note: this loop can only be used when the V.110 mode is selected in register
W00.

```
        DTE   |     |   EDRA
              |     |
              |     |
    C/105  |-----▷| C105─┐
              |     |     |
              |     |     |
    I/109  |◁-----| I109─┘
              |     |
```
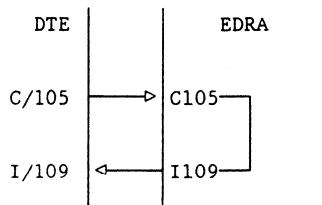
Figure 2.9.1.3-5   local testloop C—▷I

Bit LLP1: If bit LLP1 is made '1' local testloop 1 is set. In this testloop
the input T103 is inside the EDRA connected to the R104 output. The local
testloop 1 is illustrated in figure 2.9.1.3-6.

```
        DTE   |     |   EDRA
              |     |
              |     |
  ──T/103 |----->| T103─┐    SDO
              |     |     |
              |     |     |
  ──R/104 |------| R104◁─┘   SDI
              |     |
```

Figure 2.9.1.3-6   local testloop 1

2.9.1.4. Register W03

Bit NoCCITT: When the EDRA is in X.30 mode and bit NoCCITT is '0', circuit
I109 is byte timing synchronous according to CCITT recommendation X.30. The
circuit I109 will be delayed to have a change at the first 1 to 0
transition of S114 after the 1 to 0 transition of circuit B (B115). The
timing relation between B115, S114 and I109 is depicted in figure 2.9.1.4-1.

Extended data rate adaptor

I109

S114

B115
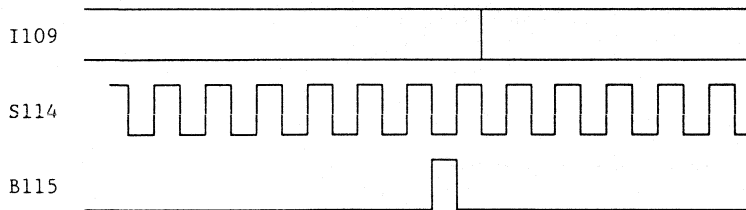
Figure 2.9.1.4-1 the timing relation between the outgoing interchange circuits when NoCCITT is set to '0'.

When the EDRA is in X.30 mode and bit NoCCITT is '1', the NOT CCITT compatible mode is selected: I109 will be changed at the 1 to 0 transition of S114 when B is 1, at this same moment the 8th databit will be clocked out on circuit R104; so I109 is one bit earlier as defined in CCITT's X.30. The timing relations when the outgoing interchange circuits are not in the CCITT compatible mode are depicted in figure 2.9.1.4-2.

I109

S114

B115
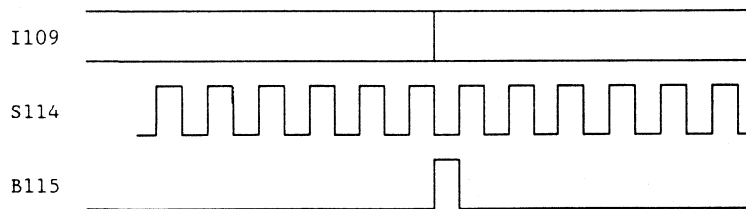
Figure 2.9.1.4-2 the timing relation between the outgoing interchange circuits when NoCCITT is set to '1'.

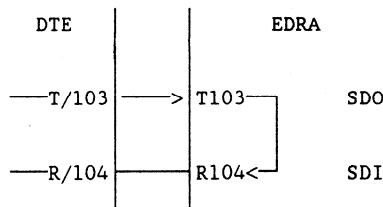Bit E7: The E7 bit is used for the data rate setting in the 10 bytes frame for user data rates > 1200 bit/s. For lower speeds this bit is internally used for multiframe synchronisation and is coded as is illustrated in table 2.9.1.4-3.

Bit FM0 and FM1: With bit FM0 and FM1 the intermediate frame speed can be selected when submultiplexing on the synchronous data interface is needed. When no submultiplexing is used, 64 kbit/s should be selected. The coding of the bits FM0 and FM1 is illustrated in table 2.9.1.4-4.

Extended data rate adaptor

FM1	FM0	intermediate data rate
0	0	8000
0	1	16000
1	0	32000
1	1	64000

Table 2.9.1.4-4 Intermediate data rate selection

Extended data rate adaptor

```
Data rate 600 bit/s:

multiframe 1 |00000000|1PPPPPPS|1PPPPPPX|1PPPPPPS|1PPPPPPS|
              |        | 111111 | 112222 | 222233 | 333333 |

              |1EEEEEE1|1PPPPPPS|1PPPPPPX|1PPPPPPS|1PPPPPPS|
              | 123456 | 444444 | 445555 | 555566 | 666666 |

multiframe 2 |00000000|1PPPPPPS|1PPPPPPX|1PPPPQQS|1QQQQQQS|
              |        | 777777 | 778888 | 888811 | 111111 |

              |1EEEEEE1|1QQQQQQS|1QQQQQQX|1QQQQQQS|1QQQQQQS|
              | 123456 | 222222 | 223333 | 333344 | 444444 |

multiframe 3 |00000000|1QQQQQQS|1QQQQQQX|1QQQQQQS|1QQQQQQS|
              |        | 555555 | 556666 | 666677 | 777777 |

              |1EEEEEE1|1QQQQQQS|1QQRRRRX|1RRRRRRS|1RRRRRRS|
              | 123456 | 888888 | 881111 | 111122 | 222222 |

multiframe 4 |00000000|1RRRRRRS|1RRRRRRX|1RRRRRRS|1RRRRRRS|
              |        | 333333 | 334444 | 444455 | 555555 |

              |1EEEEEE0|1RRRRRRS|1RRRRRRX|1RRRRRRS|1RRRRRRS|
              |        | 666666 | 667777 | 777788 | 888888 |

After four multiframes, the E7 bit changes from 1 to 0, which
indicates that three complete data bytes have been transmitted.

Data rate 1200 bit/s:

multiframe 1 |00000000|1PPPPPPS|1PPPPPPX|1PPPPPPS|1PPPPPPS|
              |        | 111122 | 223333 | 444455 | 556666 |

              |1EEEEEE1|1PPPPPPS|1PPQQQQX|1QQQQQQS|1QQQQQQS|
              | 123456 | 777788 | 881111 | 222233 | 334444 |

multiframe 2 |00000000|1QQQQQQS|1QQQQQQX|1QQQQRRS|1RRRRRRS|
              |        | 555566 | 667777 | 888811 | 112222 |

              |1EEEEEE0|1RRRRRRS|1RRRRRRX|1RRRRRRS|1RRRRRRS|
              | 123456 | 333344 | 445555 | 666677 | 778888 |

After two multiframes, the E7 bit changes from 1 to 0, which
indicates that three complete data bytes have been transmitted.
```

Table 2.9.1.4-3 Multiframe synchronisation.

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Bits SG2,SG1 and SG0. These bits are the submultiplex code bits. They
determine the bit position in the SDO timeslot where the EDRA will insert
data (see section 2.4).

SG2	SG1	SG0	bitpositions for intermediate:			
			8000	16000	32000	64000
0	0	0	0	0 1	0 1 2 3	-
0	0	1	1	2 3	4 5 6 7	-
0	1	0	2	4 5	-	-
0	1	1	3	6 7	-	-
1	0	0	4	-	-	-
1	0	1	5	-	-	-
1	1	0	6	-	-	-
1	1	1	7	-	-	-

Table 2.9.1.4-5 Submultiplex code bits

Bit SDO=1. When bit SDO=1 is set to '1', the EDRA will clamp the outgoing
data on the ssynchronous data interface to '1'.

2.9.1.5. Register W04

Bit RxGIE: Bit RxGIE bit (when set to '1') enables the URF-receiver activity
checkers (register R27) to generate interrupts. These activity checkers can
be individually enabled in register W13.

Bit TxGIE: Bit TxGIE (when set to '1') enables the URF-transmitter activity
checkers to give interrupts. These activity checkers (register R20) can be
individually enabled in register W13.

Bit OOSIE, when set to '1', enables the activity checker OOSact (register
R20) to give interrupts. The OOSstate can be read in register R22.

Bit THGIE, when set to '1', enables the URF-FIFO threshold activity checkers
to give interrupts. The activity and status of the FIFO thresholds can be
read in register R28.

Bit ICGIE (when set to '1') enables the interchange circuits activity
checkers to give interrupts. The activity checkers can be individually
enabled in registers W05 and W08. The status and activity bits of the
interchange circuits can be read in registers R21, R22, R23 and R24.

Bit MIE. When bit MIE is set to '0', all EDRA interrupts are disabled.

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2.9.1.6. Register W05

Bit SXI controls the programmable inverters on the interchange input circuits. This control is necessary to define the binary state of ON and OFF according CCITT definition or to be compatible with the DRA (PCB2320).

If SXI is made '0', the inputs have no inversion and the S- and X-bits in the synchronous data interface stream are CCITT compatible (ON=0, OFF=1). When SXI is made '1', the inputs are inverting and the EDRA is DRA compatible (ON=1, OFF=0). Bit SXI influences only the S- and X-bit definition in the 64 kbit/s data stream. The readouts and clampings of the input interchange circuits remain as in CCITT compatible mode.

Bit DTE106IE: when bit DTE106IE is set to '1', the EDRA generates an interrupt on the setting of DTE106 activity bit (register R21).

Bit MO1IE: when bit MO1E is set to '1', the EDRA generates an interrupt on the setting of MO1 activity bit (register R21).

Bit MO2IE: when bit MO2IE is set to '1', the EDRA generates an interrupt on the setting of MO2 activity bit (register R21).

Bit V108IE: when bit V108IE is set to '1', the EDRA generates an interrupt on the setting of V108 activity bit (register R21).

Bit C105IE: when bit C105IE is set to '1', the EDRA generates an interrupt on the setting of C105 activity bit (register R21).

Bit T103IE: when bit T103IE is set to '1', the EDRA generates an interrupt on the setting of T103 activity bit (register R21).

Bit R104IE: when bit R104IE is set to '1', the EDRA generates an interrupt on the setting of R104 activity bit (register R21).

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2.9.1.7. <u>Register W06</u>

Bit T103/1 and T103/0: With T103/0 and T103/1 it is possible to control
input T103. The input can be clamped (internally) to '0' or '1' or the EDRA
accepts input on lead T103. For the settings of T103/0 and T103/1 is
referred to table 2.9.1.7-1.

T103/1	T103/0	T103
0	0	EDRA accepts data on T103
0	1	T103 is internally clamped to 0
1	X	T103 is internally clamped to 1

Table 2.9.1.7-1 Settings of T103/0 and T103/1.

Bit C105/1 and C105/0: With C105/0 and C105/1 it is possible to control
input C105. The input can be clamped (internally) to '0' or '1' or the EDRA
accepts input on lead C105. For the settings of C105/0 and C105/1 is
referred to table 2.9.1.7-2.

C105/1	C105/0	C105
0	0	EDRA accepts data on C105
0	1	C105 is internally clamped to 0
1	X	C105 is internally clamped to 1

Table 2.9.1.7-2 Settings of C105/0 and C105/1.

Bit V108/1 and V108/0: With V108/0 and V108/1 it is possible to control
input V108. The input can be clamped (internally) to '0' or '1' or the EDRA
accepts input on lead V108. For the settings of V108/0 and V108/1 is
referred to table 2.9.1.7-3.

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V108/1	V108/0	V108
0	0	EDRA accepts data on V108
0	1	V108 is internally clamped to 0
1	X	V108 is internally clamped to 1

Table 2.9.1.7-3 Settings of V108/0 and V108/1.

Bit DTE106/1 and DTE106/0: With DTE106/0 and DTE106/1 it is possible to control input DTE106. The input can be clamped (internally) to '0' or '1' or the EDRA accepts input on lead DTE106. For the settings of DTE106/0 and DTE106/1 is referred to table 2.9.1.7-4.

DTE106/1	DTE106/0	DTE106
0	0	EDRA accepts data on DTE106
0	1	DTE106 is internally clamped to 0
1	X	DTE106 is internally clamped to 1

Table 2.9.1.7-4 Settings of DTE106/0 and DTE106/1.

2.9.1.8. Register W07

Bits S1, X2, S3, S4, S6, X7, S8, S9: In μC mode these bits that are transferred in the frame over the synchronous data interface, can be programmed by the microcontroller. Setting these bits is only useful when the μC-mode is selected in register W00.

note: for speeds > 38.4 kbit/s not all bits are transferred in the 4 bytes frame (see section 2.3) (it of no use programming the bits that are not transferred).

2.9.1.9. Register W08

Bits S1IE, X2IE, S3IE, S4IE, S6IE, X7IE, S8IE, S9IE. If one of these bits is set to '1' the interrupt is enabled on the related activity bit (register R23). If the related activity bit is set an interrupt is generated by the EDRA.

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2.9.1.10. Register W09

Bits R104/0 and R104/1: With R104/0 and R104/1 it is possible to control output R104. The output can be clamped to '0' or '1' or is indicating the received data bits. For the settings of R104/0 and R104/1 is referred to table 2.9.1.10-1.

R104/1	R104/0	R104
0	0	EDRA indicates on R104 the received D bits
0	1	R104 is internally clamped to 0
1	X	R104 is internally clamped to 1

Table 2.9.1.10-1 Settings of R104/0 and R104/1.

Bits DCE106/1 and DCE106/0: With DCE106/1 and DCE106/0 it is possible to control output DCE106. The output can be clamped to '0' or '1' or is indicating the X7- and/or X2-bits (see section 2.3). For the settings of DCE106/1 and DCE106/0 is referred to table 2.9.1.10-2.

DCE106/1	DCE106/0	DCE106
0	0	EDRA indicates on DCE106 the received X bits
0	1	DCE106 is internally clamped to 0
1	X	DCE106 is internally clamped to 1

Table 2.9.1.10-2 Settings of R104/0 and R104/1.

Bit V107/0 and V107/1: With V107/0 and V107/1 it is possible to control output V107. The output can be clamped to '0' or '1' or is indicating the received S1-, S3-, S6- and S8-bits (see section 2.3). For the settings of V107/0 and V107/1 is referred to table 2.9.1.10-3.

V107/1	V107/0	V107
0	0	EDRA indicates on V107 the received S bits
0	1	V107 is internally clamped to 0
1	X	V107 is internally clamped to 1

Table 2.9.1.10-3 Settings of V107/0 and V107/1.

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Bits I109/1 and I109/0: With I109/1 and I109/0 it is possible to control output I109. The output can be clamped to logic '0' or '1' or is indicating the received S9- and/or S4-bits (see section 2.3). For the settings of I109/1 and I109/0 is referred to table 2.9.1.10-4.

I109/1	I109/0	I109
0	0	EDRA indicates on I109 the received S bits
0	1	I109 is internally clamped to 0
1	X	I109 is internally clamped to 1

Table 2.9.1.10-4 Settings of I109/1 and I109/0.

2.9.1.11. Register W10

Bit SXO: Bit SXO controls the programmable inverters on the interchange output circuits. This control is necessary to program the relation between the binary values of S- and X-bits and the states (ON and OFF) of the interchange circuits. This relation can be according CCITT definition or ECMA-102 september '84 (to be compatible with the DRA (PCB2320)).

If SXO is made '0', the outputs have no inversion and the S- and X-bits in the synchronous data interface stream are interpreted according CCITT standard (ON=0, OFF=1). When SXO is made '1', the outputs are inverting and the EDRA is DRA compatible (ON=1, OFF=0). Bit SXO influences only the interpretation of the S- and X-bits in the 64 kbit/s data stream. The readouts and clampings of the input interchange circuits remain as in CCITT compatible mode.

Bit MO2: With this bit, the state of output pin MO2 can be set or reset by the micro controller. When MO2 is made '1' the output is '1' (5V), a '0' results in 0V at the MO2 output.

Bit S114=1. When this bit is set to '0', the output S114 delivers the timing signals S114 as described in section 2.3.3. When S114-1 is set to '1', the output is clamped to '1' (5V). See figure 2.9.1.11-1.

Bit B115=1. When this bit is set to '0', the output S114 delivers the timing signals B115 as described in section 2.3.3. When B115-1 is set to '1', the output is clamped to '1' (5V). See figure 2.9.1.11-1.

Bit MO1: With this bit, the state of output pin MO1 can be set or reset by the micro controller. When MO1 is made '1' the output is '1' (5V), a '0' results in 0V at the MO1 output.

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Bit TXsBr: When this bit is set '1' the EDRA generates a break condition on circuit R104 (as long as this bit is '1'). The current character that is transmitted will be corrupted while the next characters will be stored in the Tx-FIFO.
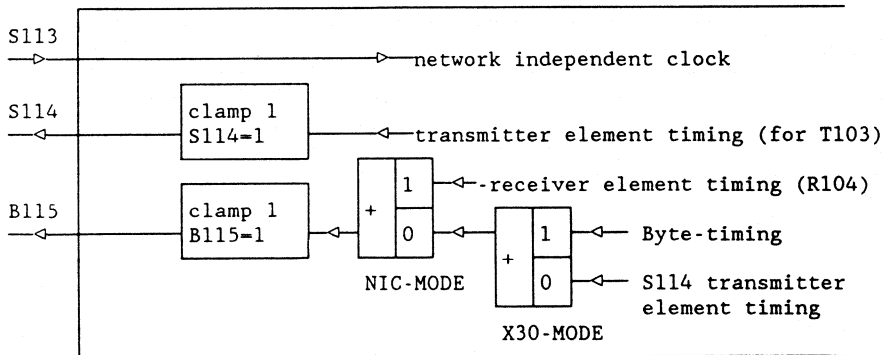

Figure 2.9.1.11-1 Interchange circuits B115 and S114.

2.9.1.12. Register W11

Bit CC0 - CC7: Bit CC0 - CC7 are the command code bits. With these bits data settings of the URF transmitter/receiver blocks can be set. In table 2.9.1.12-1 the settings of CC0 - CC7 are illustrated.

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CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	action
1	-	-	-	-	0	-	1	reset FIFOs
0	-	0	-	0	-	0	1	5 bits/character
0	-	0	-	0	-	1	0	7 bits/character
0	-	0	-	0	-	1	1	8 bits/character
0	-	0	0	1	0	0	-	none parity
0	-	0	0	1	1	0	0	odd parity
0	-	0	0	1	1	0	1	even parity
0	-	0	0	1	1	1	0	space parity
0	-	0	0	1	1	1	1	mark parity
0	-	0	1	1	0	1	0	1 stopbit
0	-	0	1	1	0	1	1	2 stopbits *4)
1	-	-	-	-	1	-	0	Tx sends one X-ON (on lead R104)
1	-	-	-	-	1	-	1	Tx sends one X-OFF (on lead R104)
0	-	1	0	-	0	0	0	Rx X-ON filter OFF (on lead T103) *0)
0	-	1	0	-	0	0	1	Rx X-ON filter ON (on lead T103) *1)
0	-	1	0	-	0	1	0	Rx X-OFF filter OFF (on lead T103) *0)
0	-	1	0	-	0	1	1	Rx X-OFF filter ON (on lead T103) *1)
0	-	1	0	-	1	-	0	auto XON/XOFF (on lead T103 and R104)
0	-	1	0	-	1	-	1	auto circuit 106 *3)
0	-	1	1	-	0	0	1	Tx transmit enabled (lead R104) *0)
0	-	1	1	-	0	0	0	Tx transmit disabled (lead R104)
0	-	1	1	-	0	1	1	Tx transmit enabled, controlled by the local DTEs lead T103 X-ON/X-OFF *1)
0	-	1	1	-	1	0	1	Rx transmit enabled (synchronous data interface) *0)
0	-	1	1	-	1	0	0	Rx transmit disabled (synchronous data interface)
0	-	1	1	-	1	1	-	Rx transmit enabled, controlled by the remote EDRAs X-bit *2)

Figure 2.9.1.12-1   Selections for URF (UART/RA0/Flowcontrol).

*0) automatic selected at any write action in register W00.
*1) automatic selected in auto X-ON/X-OFF mode if flowcontrol is selected in register W00.
*2) automatic selected at selection of flowcontrol in register W00.

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*3) there is always an automode selected. This means that for other
    modes than the flowcontrol mode, lead DCE106 should be coupled
    directly to the incoming X-bits, the auto X-ON/X-OFF must be selected,
    in combination with Rx-threshold level setting at FF-Hex, unless auto
    X-ON/X-OFF is wanted for local flowcontrol purposes.
*4) in two stopbit mode, the receiver checks on two stop-elements

Note 1: bits/char, partity and number of stopbit: no default setting, must
all be set when using URF (mode 1B, 1C and 1D), For mode 2, 3A, 3B and 3C
(only 8 bits character has to be programmed).

Note 2: Tx send one X-ON/X-OFF: after the current character is transmitted,
a X-ON or X-OFF will be transmitted to the local DTE. This can be usefull
when in using RA0. When this feature is used in flowcontrol mode (mode 1C),
one should realise that this manual X-ON/X-OFF will disturb the auto
generated X-ON/X-OFF or DTE106.

Note 3: Rx X-ON/X-OFF filters, AUTO X-ON/X-OFF/ AUTO DCE106: one of these
modes must be set. See chapter 2.5.3.

Note 4: Tx and Rx transmit enabled/disabled: see chapter 2.5.3.

2.9.1.13. Register W12

Bits TH1A1 - TH1A4: bits TH1A1 - TH1A4 contain the threshold level 1 of the
receiver FIFO (see section 2.5.3.1). It indicates an odd addresses (with
TH1A1 -TH1A4 address 1 upto 31 can be selected the least significant bit is
always 1).

Bits TH2A1 - TH2A4: bits TH2A1 - TH2A4 contain the threshold level 2 of the
receiver FIFO (see section 2.5.3.1). It indicates an odd addresses (with
TH2A1 -TH2A4 address 1 upto 31 can be selected the least significant bit is
always 1).

2.9.1.14. Register W13

Bit XonXoffIE: This bit enables the URF receiver X-ON and X-OFF activity
bits (see register R26) to generate interrupts.

Bit TxAllSeIE: This bit enables the EDRA to generate an interrupt when
activity bit Txallsent (register R20) becomes '1'.

Bit TxFIFOeIE: This bit enables the EDRA to generate an interrupt when the
bit TxFIFOempty state (register R20) becomes '1'.

Bit RXChAvIE: This bit enables the EDRA to generate an interrupt if the
char.av activity (register R27) becomes '1'.

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Bit Rx/TxOfIE: This bit enables the EDRA to generate an interrupt at the moment the overflw act. bit (register R27) or the Tx FIFO overfl. activity bit (register R20) become '1'.

Bit RxBreakIE: When this bit is made '1' the EDRA generates an interrupt when the break state bit (register R27) becomes '1'.

Bit RxParIE: When this bit is made '1' it enables the EDRA to generate an interrupt at the moment the frmerr activity bit (register R27) is '1'.

Bit RxFrEr: When this bit is set ('1') the EDRA genrates an interrupt at the moment the frmerr activity bit (register R27) is set (has become '1').

2.9.1.15. Register W14

Bits TH1A1 - TH1A4: bits TH1A1 - TH1A4 contain the threshold level 1 of the transmitter FIFO (see section 2.5.3.1). It indicates an odd addresses (with TH1A1 -TH1A4 address 1 upto 31 can be selected the least significant bit is always 1).

Bits TH2A1 - TH2A4: bits TH2A1 - TH2A4 contain the threshold level 2 of the transmitter FIFO (see section 2.5.3.1). It indicates an odd addresses (with TH2A1 -TH2A4 address 1 upto 31 can be selected the least significant bit is always 1).

2.9.1.16. Register W15

The data can be written by microcontroller to the UART, via this write register. Before a byte can be written, the TxFIFOoverfl activity bit in register R20 must be '0'.

2.9.1.17. Register W16

In this register the flowcontrol X-ON character code can be downloaded.

2.9.1.18. Register W17

In this register the flowcontrol X-OFF character code can be downloaded.

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2.9.2. Registers R20-R28

General activity/state register:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R20	Tx FIFO overfl. act.	Tx FIFO empty state	Tx all sent act.	-	IC group act.	TH group act.	OOS act.	Rx group act.

Table 2.9.2-1 Bit assignment;register R20.

Input interchange circuits activity indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R21	R104ACT 0-1/1-0	T103ACT 0-1/1-0	C105ACT 1-0	C105ACT 0-1	V108ACT 1-0	V108ACT 0-1	MI1/MI2 0-1/1-0	DTE106 0-1/1-0

Table 2.9.2-2 Bit assignment;register R21.

Input interchange circuits status indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R22	-	OOS state	C105	-	V108	MI2	MI1	DTE106

Table 2.9.2-3 Bit assignment;register R22.

Output interchange circuits activity indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R23	S9 ACT 0-1/1-0	S8 ACT 0-1/1-0	X7 ACT 0-1/1-0	S6 ACT 0-1/1-0	S4 ACT 0-1/1-0	S3 ACT 0-1/1-0	X2 ACT 0-1/1-0	S1 ACT 0-1/1-0

Table 2.9.2-4 Bit assignment;register R23.

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Output interchange circuits status indications:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R24	S9	S8	X7	S6	S4	S3	X2	S1
R25	E7	E6	E5	E4	E3	E2	E1	-

Table 2.9.2-5 Bit assignment;register R24 and R25.

UART receive buffer:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R26	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0

Table 2.9.2-6 Bit assignment;register R26.

URF receiver state/activity register:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R27	Xon det act.	Xoff act.	FIFOemp state	frm.err act.	par.err act.	break state	overflw act.	char.av act

Table 2.9.2-7 Bit assignment;register R27.

FIFO threshold status and activity register:

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R28	Tx TH1 state	Tx TH2 state	Tx TH1 act.	Tx TH2 act.	Rx TH1 state	Rx TH2 state	Rx TH1 act.	Rx TH2 act.

Table 2.9.2-8 Bit assignment;register R28.

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2.9.2.1. Register R20

Bit Rx group act.: Receiver Group activity (URF-bit). This bit indicates
that one of more receiver activity bits have become '1'. This activity-bits
can not be read but the status bits that caused the activity can be read in
register R27. After this read cycle the activity bits will be reset and the
INTN lead goes HIGH (non active).

OOSact.: 64 kbit/s channel Out Of Synchronisation. This activity bit
indicates the in-synchronisation to out-synchronisation transition of the
synchronisation mechanism in the CS. This for all speed-setting in W01,
exept for synchronous 56 and 64 kbit/s. For these speeds, this bit will
always be '0' (in synchronisation). After readout the activity bit will be
reset. The status bit OOS state in register R22 indicates the real time
state of synchronisation.

While synchronising, the incoming datastream on SDI is checked for frame
synchronisation bits. If they don't appear on the expected position in the
frame, this can have two causes: The clockunit must be presetted to the
right value or one of more frame synchronisation bits have been distorted.

For the ten bytes frame:

The EDRA gives out of synchronisation after three consecutive incorrect
multiframes (with one or more errors per multiframe) and starts searching
for the right timing:
-After receiving the eight zero frame bits the clockunit is preset to the
right value,
-If the following frame-bits in that multiframe are received correctly,
the EDRA is in synchronisation and OOS state in register R22 will be reset.

-If they are not all correct the OOS bit remains '1' and the EDRA will
search for the next 8 zero frame-bits.

For the four bytes frame:

The EDRA gives out of synchronisation after three consecutive incorrect
frames of 4-bytes (with one or more errors per frame) and starts searching
for the right timing:

-The incoming data on the synchronous data interface have correct
octet-orientation.
-After receiving the 1011-pattern in the frame synchronisation bits, the
EDRA is in synchronisation and the OOS state bit will be reset.
-If they are not all correct the OOS state bit remains '1' and the EDRA will
continue searching for the synchronisation pattern.

Bit TH group act.: Threshold group activity bit. This bit indicates that
one of the receiver or transmitter threshold activity checkers is active
('1').

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Bit IC group act.: Interchange circuits group activity. This bit indicates that one or more of the IC activity checkers are active ('1').

Bit Tx all sent act.: Tx all sent activity bit. This bit becomes '1' when all characters have completely cleared the transmitter. It will be reset after reading register R20.

Bit Tx FIFO empty state: Tx FIFO empty state bit. When this bit is '1', the Tx FIFO contains no more data.

Bit Tx FIFO overfl. act.: When this bit becomes '1', it indicates that a Tx FIFO overflow has occurred. This bit is reset after reading register R20.

2.9.2.2. Register R21

Bit DTE1060-1/1-0: Activity check bit on input DTE106. If any signal changes on this input pin occur, this bit is set '1'.

MI1/MI20-1/1-0: Activity check bit on inputs MI1 and MI2. If any signal changes on one of these input pins occur, this bit is set '1'.

Bit V108act0-1: Activity check bit on input V108. If any signal changes from 0 to 1 occur on this input pin, this bit is set '1'.

Bit V108act1-0: Activity check bit on input V108. If any signal changes from 1 to 0 occur on this input pin, this bit is set '1'.
Bit C105act0-1: Activity check bit on input C105. If any signal changes from 0 to 1 occur on this input pin, this bit is set '1'.

Bit C105act1-0: Activity check bit on input C105. If any signal changes from 1 to 0 occur on this input pin, this bit is set '1'.

Bit T103ACT0-1/1-0: Activity check bit on input T103. If any signal changes on this input pin occur, this bit is set '1'.

Bit R104ACT0-1/1-0: Activity check bit on output R104. If any signal changes on this input pin occur, this bit is set '1'.

2.9.2.3. Register R22

Bit DTE106, MI1, MI2, V108, C105: These bits indicate the actual state of the input they are named after. If the input is HIGH (5V) the bit is '1'. If the inupt is LOW (0V) the bit is '0'.

Bit OOS state: It gives the actual state of the synchronisation system of the EDRA. This for all user data rates, exept for synchronous 56 and 64 kbit/s. For these speeds, this bit is always '0' (in synchronisation).

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2.9.2.4. Register R23

Bit S9 ACT 0-1/1-0, S8 ACT 0-1/1-0, X7 ACT 0-1/1-0, S6 ACT 0-1/1-0, S4 ACT 0-1/1-0, S3 ACT 0-1/1-0, X2 ACT 0-1/1-0, S1 ACT 0-1/1-0: These bit are activity bits and are set to '1' is any signal changes occur in the S and X-bits of the incoming frame on pin SDI (synchronous data input).

In case of a 4 bytes frame only S1/X2/S3/S4 contain valid information.

2.9.2.5. Register R24

Bits S1, X2, S3, S4, S6, X7, S8, S9: contain the actual state of the bits they are named after. The information in these bits is filled in by the remote EDRA.

In case of a 4 bytes frame only S1/X2/S3/S4 contain valid information.

2.9.2.6. Register R25

Bits E1, E2, E3, E4, E5, E6, E7: In every 10 bytes multi-frame (for speeds not exeeding 38400 bit/s), 7 E-bits are available. The information filled in by the remote subscriber is received in these bits.

These bits are only applicable in a 10 bytes frame.

2.9.2.7. Register R26

Bits RX0 - RX7: Data bytes of the UART receive buffer can be read out of this register.

2.9.2.8. Register R27

Bit char.av.act.: The character available activity bit indicates that a character can be read out of the UART Rx buffer. An interrupt will be given, if the interrupt source in the EDRA is enabled in register W13. Character available is an activity bit, and will be reset after reading register R27.

Bit overflw act.: Receive FIFO overflow error activity bit. This bit indicates that the receive FIFO has an overflow. This bit is an activity bit, and will be reset after reading register R27. If enabled in W13, an interrupt will be given by the EDRA when this bit is set (become '1').

Bit break state. This bit is set ('1') when a break sequence has been detected, and will last as long as this condition is present, If enabled, in register W13 an interrupt will be given by the EDRA at the moment this bit is set.

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Bit par.err.act.: Parity Error activity bit. When parity is enabled, this bit is set for the characters whose parity do not match the programmed sense. It is an activity bit, and will be reset after reading register R27. It pops with the data, so must be read before reading the UART receive buffer (register R26). When the parity error bit is set, and the interrupt is enabled in register W13, an interrupt will be given.

Bit frm.err act. This bit is set ('1') when the stop bit is not found. It is an activity bit, and will be reset after reading register R27. It pops with the data. When enabled in register W13 the EDRA generates an interrupt when this bit is set.

Bit FIFOemp state: Rx FIFO empty. This is a state bit and is set when no characters are left in the 32 bytes Rx-FIFO.

Bit Xoff act.: Rx X-OFF detection. This activity bit is set when an incoming character on lead T103 is equal to the character written in register W17. This bit is reset after reading register W27.

Note: The incoming character may not contain frame or parity error.

Bit Xon det act.: Rx X-ON detection. This activity bit is set when an incoming character on lead T103 is equal to the character written in register W16. The bit is reset after reading register W27.

Note: The incoming character may not contain frame or parity error.

2.9.2.9. Register R28

Bit Rx TH2 act.: It indicates the 0/1 transition of the receiver TH2 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Rx TH1 act.: It indicates the 0/1 transition of the receiver TH1 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Rx TH2 state: When this bit is '1', the contents of this FIFO is equal or passed the receiver FIFO TH2 (lower) threshold.

Bit Rx TH1 state: This bit indicates the state of the receiver FIFO. When this bit is '1', the contents of this FIFO is equal or passed the TH1 (upper) threshold.

Bit Tx TH2 act.: It indicates the 0/1 transition of the transmitter TH2 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

Bit Tx TH1 act.: It indicates the 0/1 transition of the transmitter TH1 state. If enabled in register W04, the EDRA generates an interrupt on the setting of this bit.

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Bit Tx TH2 state: When this bit is '1', the contents of this FIFO is equal or passed the transmitter FIFO TH2 (lower) threshold.

Bit Tx TH1 state: This bit indicates the state of the transmitter FIFO. When this bit is '1', the contents of this FIFO is equal or passed the TH1 (upper) threshold.

3. Testability

The EDRA has two test modes on board: A boudary scan test and a possiblity to make all output pins high-Z. These test modes can be set by three control pins: SCC, BSE and BSI. With these pins the next modes are selectable:

BSI	BSE	SCC	MODE
x	0	0	normal
0	1	1	high-Z
x	1	0	boundary shift

Table 3-1 Testmode setting

For testing after PCB assembly two features are interesting: the high-Z mode and the boundary scantest. In the high-Z mode, all chip outputs are high impedance, which will make testing of other devices mounted on the PCB easier.
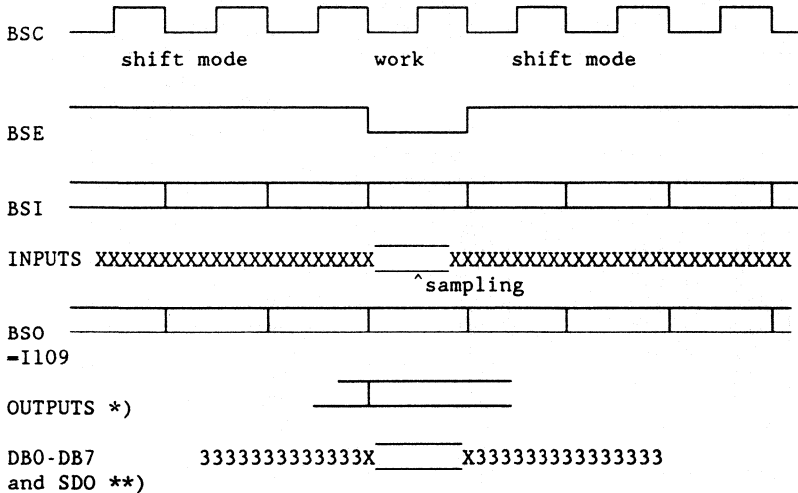
The boundary scantest enables to check the connections between the chippads and the PCB. The boundary test is a method to check the connections of the chip-pads to the PCB. In the boundary scan mode, all output pins can be set, and all input pins can be sensed, via the boundary scanline.

Testvalues should be driven from electrical specification.

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In the following figure the functional timing is illustrated in the boudary
scan testmode:

```
BSC  ──┐ ┌─┐ ┌─┐ ┌─┐ ┌─┐ ┌─┐ ┌─┐ ┌─┐ ┌─┐ ┌──
       └─┘ └─┘ └─┘ └─┘ └─┘ └─┘ └─┘ └─┘ └─┘
         shift mode        work      shift mode
```

```
BSE  ─────────────────────────┐       ┌──────────────
                              └───────┘
```

```
BSI  ──────┐ ┌───┐ ┌───┐ ┌───┐ ┌───┐ ┌───┐ ┌───┐ ┌───
```

```
INPUTS XXXXXXXXXXXXXXXXXXXXXXXX_____XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
                                ^sampling
```

```
BSO  ──────┐ ┌───┐ ┌───┐ ┌───┐ ┌───┐ ┌───┐ ┌───┐ ┌───
```
−I109

```
OUTPUTS *)                  ────┐     ┌────
                               ─┴─────
```

DB0-DB7   3333333333333X_____X333333333333333
and SDO **)

*)   except DB0 - DB7 and SDO
**)   High-Z during shift, in workmode dependent of B20/B21 see table 3.3

Figure 3.2 Functional timing in boundary-scan mode.

In the shift mode, BSE=1, the databus and the SDO pin are high-Z. In the
work cycle, where inputs are sampled in the scanline, and outputs are
forced, the direction of the databus and the mode of the SDO pin is
determined by two boundary chain elements: B01 and B02;

control	behaviour in workcycle
B01 = 0 = 1	DB0 - DB7 are high-Z, databus in inputmode DB0 - DB7 in output mode from chain elements B09- B16
B02 = 0 = 1	HWO is high-Z HWO is in output mode, from chain element B19

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Boundaryscan chainorder:

NR.	NAME	SHIFT FROM	WORK DATA IN	WORK DATA OUT	
1	B01	BSI-pin	T103	PQ01 (data bus)	*
2	B02	B01	SCC	PQ02 (synchr. data interface)	*
3	B03	B02	internal CQ11	
4	B04	B03	internal CQ13	
5	B05	B04	SCLK	
6	B06	B05	MCLK	
7	B07	B06	RDN	
8	B08	B07	WRN	
9	B09	B08	DB0	DB0
10	B10	B09	DB1	DB1
11	B11	B10	DB2	DB2
12	B12	B11	DB3	DB3
13	B13	B12	DB4	DB4
14	B14	B13	DB5	DB5
15	B15	B14	DB6	DB6
16	B16	B15	DB7	DB7
17	B17	B16	CSN	INTN
18	B18	B17	ALE	
19	B19	B18	FSX	SDO
20	B20	B19	FSR	
21	B21	B20	SDI	B115
22	B22	B21	S113	MI2
23	B23	B22	V108	MO2
24	B24	B23	MI1	V107
25	B25	B24	MI2	S114
26	B26	B25	DTE106	DCE106
27	B27	B26	C105	R104
28	B28	B27		I109 = BSO

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4. DC characteristics

4.1. Ratings

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	-0.5	7.0	V
DC input diode current	$V_I< -0.5$ or $V_I> Vdd+0.5$	$\pm I_{IK}$	-	tbf	mA
DC output diode current	$V_O< -0.5$ or $V_O> Vdd+0.5$	$\pm I_{OK}$	-	tbf	mA
DC output sink current	$-0.5 <V_O< Vdd + 0.5$	$\pm I_O$	-	tbf	mA
DC output source current	$-0.5 <VO< Vdd + 0.5$	$\pm IO$	-	tbf	mA
DC V_{DD} current		$\pm I_{DD}$	-	tbf	mA
DC ground current		$\pm I_{GND}$	-	tbf	mA
Voltage on any pin		V_n	tbf	tbf	V
Storage temperature range		T_{stg}	tbf	tbf	^0C
Operating ambient temperature range		T_{amb}	-10	+75	^0C
Total power dissipation		P_{tot}	-	40	mW

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4.2. <u>DC characteristics</u>

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	4.5	5.5	V
Inputs					
Threshold voltage positive-going	$4.5 < V_{DD} < 5.5$ V	V_{T+}	-	2.0	V
negative-going	$4.5 < V_{DD} < 5.5$ V	V_{T-}	0.8	-	V
Input leak-age current	$0 < V_I < Vdd$	I_{IL}	-	1.0	uA
Outputs (except SDO & DB0..7, INTN)					
Output volt-age LOW	$V_{DD} = 5$ V $I_{OL} = 2.0$ mA	V_{OL}	-	0.4	V
Output volt-age HIGH	$VDD = 5$ V $-IOH = 2.0$ mA	V_{OH}	4.0	-	V
3-state OFF current	$0 < V_O < V_{DD}$ $I_O = 0$	$\pm I_{OZ}$	-	10	μA
Outputs (SDO,DB0..7)					
Output volt-age LOW	$V_{DD} = 5$ V $I_{OL} = 4.0$ mA	V_{OL}	-	0.4	V
Output volt-age HIGH	$VDD = 4.5$ V $-IOH = 4.0$ mA	V_{OH}	4.0	-	V
3-state OFF current	$0 < V_O < V_{DD}$ $I_O = 0$	$\pm I_{OZ}$	-	10	μA
Outputs (INTN)					
Output volt-age LOW	$V_{DD} = 5$ V $I_{OL} = 2.0$ mA	V_{OL}	-	0.4	V

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5. <u>AC Characteristics</u>

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance		C_I	-	tbf	pF
Input/ Output capacitance		$C_{I/O}$	-	tbf	pF
Output capacitance		C_O	-	tbf	pF

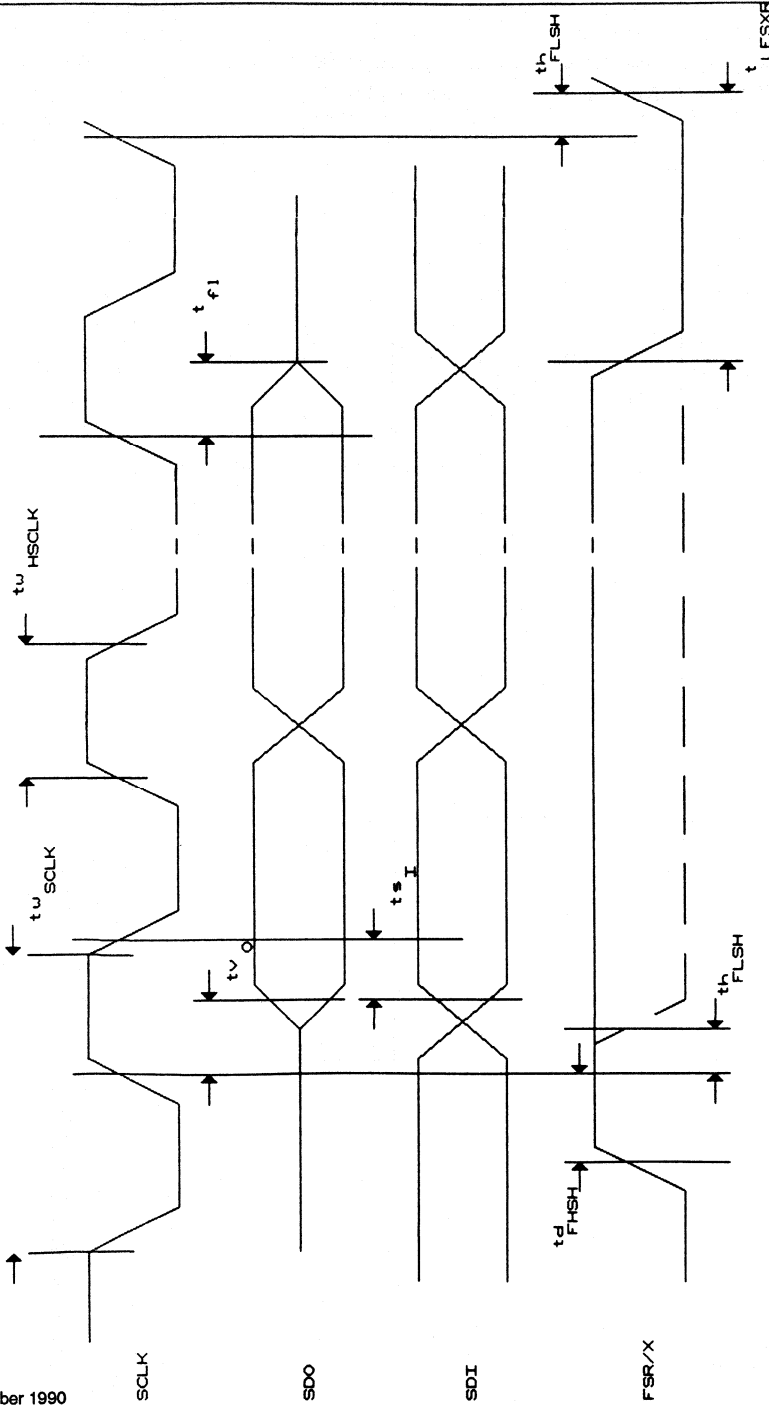Timing measurements are specified for V_{il} at 0.4 and V_{ih} at 4.0 V, V_{ol} at 20% and V_{oh} at 80% of V_{DD}.

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Synchronous data interface					
FSX/R HIGH to SCLK HIGH		td_{FHSH}	100	-	ns
hold time FSX/R LOW after SCLK HIGH		th_{FLSH}	0	-	ns
hold time FSX/R HIGH after SCLK HIGH		th_{FHSH}	0	-	ns
FSX/R LOW time		t_{LFSXR}	tw_{SCLK}	-	
SDI data set up time		ts_I	100	-	ns
SDO valid after SCLK HIGH		tv_O	-	50	ns

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Synchronous data inter-face					
SDO floating after SCLK		t_{fl}	-	20	ns
SCLK period		tw_{SCLK}	488 (ns)	15.6	μs
SCLK HIGH time		t_{HSCLK}	50	-	ns

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface					
V.110 mode without NIC					
T103					
data set up time		ts_T	100	-	ns
data hold time		th_T	0	-	ns
C105/V108 DTE106					
data set up time		ts_{CDTEV}	100	-	ns
data hold time		th_{CDTEV}	0	-	ns
R104					
data valid after S114 LOW		tv_R	100	-	ns
I109/V107 DCE106					
data valid after S114 LOW		tv_{IVDCE}	100	-	ns

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface V.110 mode with NIC T103 data valid after S113 LOW		tv_T	100	-	ns
C105/V108 DTE106 data set up time		ts_{CDTEV}	100	-	ns
R104 data valid after B115 LOW		tv_R	100	-	ns
I109/V107 DCE106 data valid after S114 LOW		tv_{IVDCE}	100	-	ns

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface					
V.110 mode asynchr.					
C105/V108 DTE106					
data set up time		ts_{CDTEV}	100	-	ns
data hold time		th_{CDTEV}	0	-	ns
I109/V107 DCE106					
data valid after S114 LOW		tv_{IVDCE}	100	-	ns

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S114

C106/DTE106/V108

BC

th CDTEV

ts CDTEV

I109/V107/DCE108

tv IVDCE
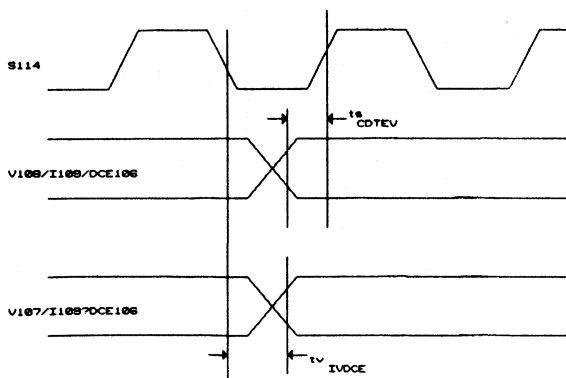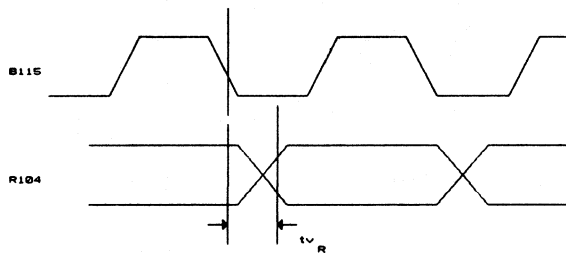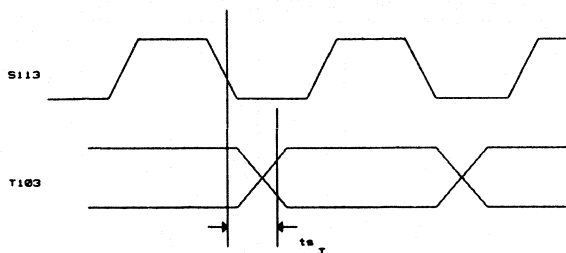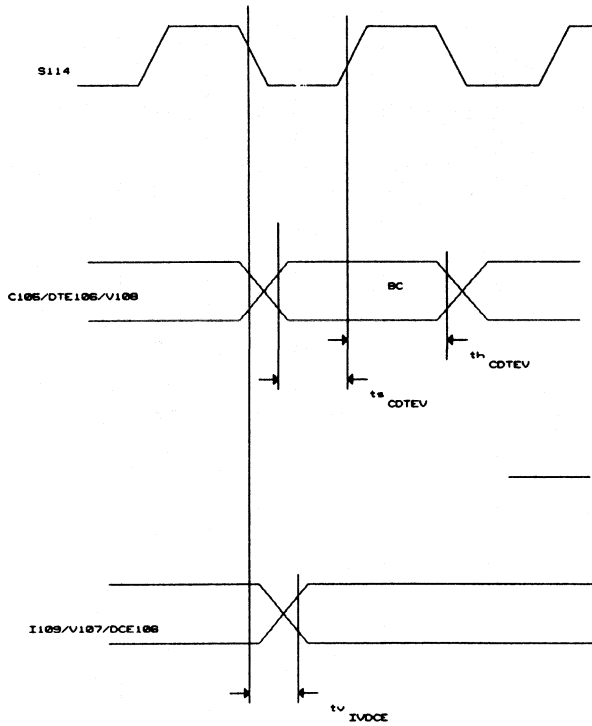
Title		
V.110 mode (1B,1C,1D) asynchronous		
Size	Document Number	REV
B	1.0	
Date: February 23, 1989	Sheet	of	1

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Interchange Interface					
X.30 mode					
T103					
data set up time		ts_T	100	-	ns
data hold time		th_T	0	-	ns
C105 DTE106					
data set up time		ts_C	100	-	ns
data hold time		th_C	0	-	ns
R104					
data valid after S114 LOW		tv_R	100	-	ns
I109					
data valid after S114 LOW		tv_I	100	-	ns

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Clock circuit					
MCLK LOW time		t_{whcl}	190	290	ns
MCLK HIGH time		t_{wlcl}	190	290	ns
SCLK transition after MCLK LOW		t_{SLML}	20		ns
SCLK transition before MCLK LOW		t_{SHML}	20		ns

Extended data rate adaptor
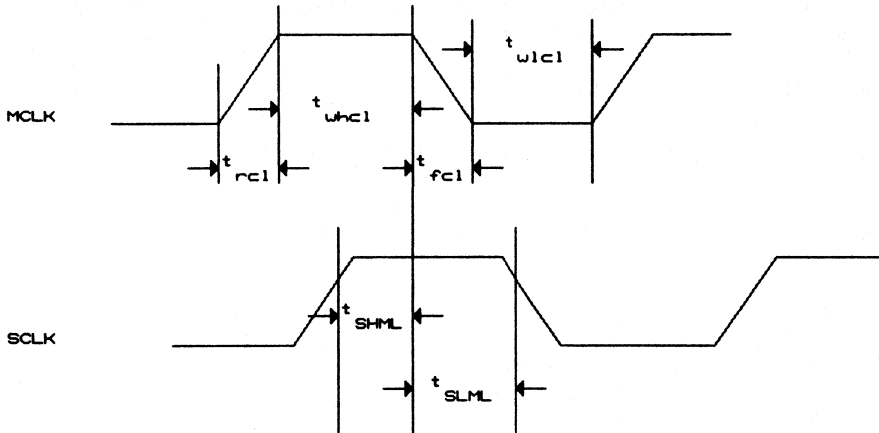
PCB2325

Title		
	MCLK and SCLK	
Size	Document Number	REV
A		
Date: February 22, 1989	Sheet	of

Extended data rate adaptor   PCB2325

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Microcontroller bus					
ALE pulse width		tw_A	100	-	ns
Data bus read cycle					
Address set up time		ts_A	55	-	ns
Address hold time		th_A	10	-	ns
RDN pulse width		tw_R	200	-	ns
Read access time	Cl = 200pF	ta_R	-	200	ns
Data hold time		th_D	10	-	ns
Time from RDN HIGH to ALE LOW		td_{RA}	1	-	μs
CSN LOW before RDN LOW		t_{CLRL}	50	-	ns
CSN HIGH before RDN HIGH		t_{CHRH}	0	-	ns
Bus floating after read		t_{fl}	-	75	ns
Time between two RDN (R 26 access)		t_{RR}	2	-	μs

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PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Microcon-troller bus					
ALE pulse width		tw_A	100	-	ns
Data bus write cycle					
Address set up time		ts_A	55	-	ns
Address hold time		th_A	10	-	ns
WRN pulse width		tw_W	100	-	ns
Data set up time		ts_D	155	-	ns
Data hold time		th_D	0	-	ns
Time from WRCEN HIGH to ALE LOW		td_{WA}	10	-	ns
CSN LOW before WRN LOW		t_{CLWL}	50	-	ns
CSN HIGH after WRN HIGH		t_{CHWH}	0	-	ns
Time between two WRN (W 15 access)		t_{WW}	2	-	μs

Extended data rate adaptor

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Extended data rate adaptor   PCB2325

Appendix A   sample moments and state changes of the interchange circuits

TRANSMITTER:
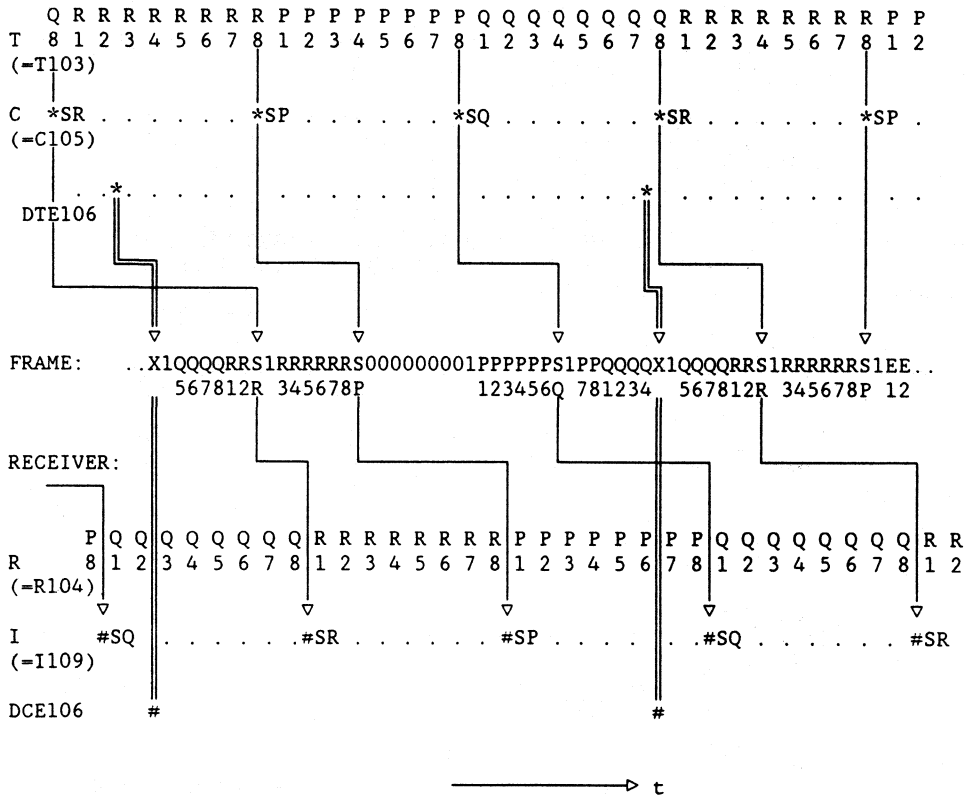
```
      Q R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R R R R R R R P P
T     8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2
(=T103)

C     *SR . . . . . . *SP . . . . . *SQ . . . . . . *SR . . . . . *SP .
(=C105)

              . .*. . . . . . . . . . . . . . . .*. . . . . . . . . . .
 DTE106

                  ▽       ▽       ▽             ▽     ▽       ▽       ▽
 FRAME:    ..X1QQQQRRS1RRRRRRS000000001PPPPPPS1PPQQQQX1QQQQRRS1RRRRRRS1EE..
               567812R 345678P         123456Q 781234  567812R 345678P 12

RECEIVER:

          P Q Q Q Q Q Q Q Q R R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R
R         8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2
(=R104)
          ▽         ▽               ▽             ▽               ▽
I     #SQ . . . . . .#SR . . . . . . #SP . . . . . .#SQ . . . . . . #SR
(=I109)

DCE106    #                                 #
```

```
                    ──────────▷ t
```

           * sample moment of the interchange circuit
           # change point of the interchange circuit

           note1: When bit repetition is used (600 and 2400 bit/s) the value
                     of last sample of the interchange circuits is repeated
                     in the data bits, the S- and X-bits till a new sample is
                     made (see appendix A, figure A-1.b and figure A-1.d).

Figure B-1 Sample moments and change points of the interchange circuit C,
             DTE106, DCE106 and I using a 10-bytes frame (rec. X.30)

Extended data rate adaptor

```
TRANSMITTER:

T
(=T103)
     Q R R R R R R P P P P P P P P P Q Q Q Q Q Q Q Q R R R R R R R R P P
     8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2

C          . . . . . *SP . . . . . . *SQ . . . . . . *SR . . . . . . *SP
(=C105)

DTE106                                              *

                          ▽        ▽        ▽         ▽        ▽
FRAME:              ...1RRRRRRS1PPPPPPPS0PPQQQQX1QQQQRRS1RRRRRRS1...
                       345678P 123456Q 781234  567812R 345678P
RECEIVER:


R                       R R R R R R R R P P P P P P P P Q Q Q Q Q Q Q Q R R
(=R104)                 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8 1 2

                        ▽              ▽                ▽                 ▽
I                       #SR . . . . . #SP . . . . . . #SQ . . . . . #SR .
(=I109)

DCE106                                                 #


                              ──────────▷ t


        * sample moment of the interchange circuit
        # change point of the interchange circuit


    Figure B-2 Sample moments and change points of the interchange circuit C,
              DTE106, DCE106, IA and I using a 4-bytes frame (rec. X.30)
```
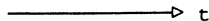
Extended data rate adaptor PCB2325

TRANSMITTER:

```
D   D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D
    4 4 4 4 4 4 4 4 4 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2
    0 1 2 3 4 5 6 7 8                 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6

S1                              *
X2                                              *
S3                                                *
S4
S6
X7        *
S8  *
S9              *

          ▽       ▽       ▽           ▽       ▽       ▽       ▽

FRAME   ..X1DDDDDDS1DDDDDDS000000001DDDDDDS1DDDDDDX1DDDDDDS1DDDDDDS1EE..
        7 3334448 4444449              1234561 7891112 1111113 1222224 12
          789012  345678                        012   345678  901234

RECEIVER:

D   D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D
    3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1
    2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8               ▽ ▽ 0 1 2 3 4 5 6 7 8

S1                                                  # #
X2                                                                    ▽
S3                                                                    #
S4
S6  #
X7  #                  ▽
S8                       #                    ▽
S9                                            #

                      ─────────────> t
```

* sample moment of the interchange circuit
# change point of the interchange circuit

note1: When bit repetition is used (600, 1200 and 2400 bit/s) the
       value of last sample of the interchange circuits is repeated
       in the data bits, the S- and X-bits till a new sample is
       made (see appendix A, figure A-1.b, A-1.c, A-1.d).

Figure B-3 Sample moments and change points of the interchange circuit 105,
       DTE106, 108 using a 10-bytes frame (rec. V.110)

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TRANSMITTER:

```
D  D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D D
   1 1 1 1 2 2 2 2 2 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 2 2 2 2 2 1 2
   6 7 8 9 0 1 2 3 4               0 1 2 3 4 5 6 7 8 9 0 1 2 3 4

S1                               *
X2                                                *
S3                                                *
S4                  *                                                        *

FRAME            ...1DDDDDDS1DDDDDDS0DDDDDDX1DDDDDDS1DDDDDDS1...
                    1222224 1234561 7891112 1111113 1222224
                    901234          012  345678  901234

RECEIVER:

D                    D D D D D D D D D D D D D D D D D D D D D D D D D
                     1 1 1 2 2 2 2 2 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1
                     7 8 9 0 1 2 3 4               0 1 2 3 4 5 6 7 8

S1                                               #
X2                                               #
S3                                                            #
S4                     #
```
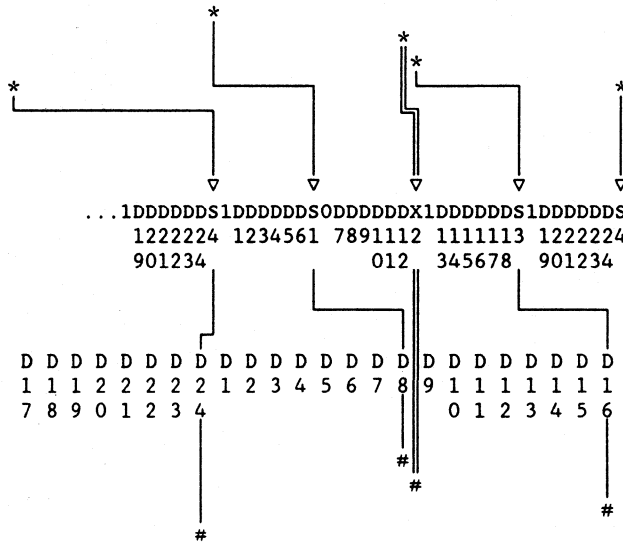
                              ─────────────▷ t

    * sample moment of the interchange circuit
    # change point of the interchange circuit

Figure B-4 Sample moments and change points of the interchange circuit 105,
          108, DTE106 using a 4-bytes frame (rec. V.110)

Extended data rate adaptor   PCB2325

Appendix B frame formats

OCTET	BIT NUMBER							
	one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1 /P1	D2 /P2	D3 /P3	D4 /P4	D5 /P5	D6 /P6	S1/SQ
two	1	D7 /P7	D8 /P8	D9 /Q1	D10/Q2	D11/Q3	D12/Q4	X
three	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
four	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D25/P1	D26/P2	D27/P3	D28/P4	D29/P5	D30/P6	S6/SQ
seven	1	D31/P7	D32/P8	D33/Q1	D34/Q2	D35/Q3	D36/Q4	X
eight	1	D37/Q5	D38/Q6	D39/Q7	D40/Q8	D41/R1	D42/R2	S8/SR
nine	1	D43/R3	D44/R4	D45/R5	D46/R6	D47/R7	D48/R8	S9/SP

Figure B-1.a Frame format of the intermediate datastream for synchronous
             user data rates when no bit repetition is used (4800, 9600,
             19200 bit/s) and frame format on the terminal highway for the
             synchronous user data rate of 38400 bit/s (V.110/X.30).

OCTET	BIT NUMBER							
	one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1 /P1	D1 /P1	D2 /P2	D2 /P2	D3 /P3	D3 /P3	S1/SP
two	1	D4 /P4	D4 /P4	D5 /P5	D5 /P5	D6 /P6	D6 /P6	X
three	1	D7 /P7	D7 /P7	D8 /P8	D8 /P8	D9 /Q1	D9 /Q1	S3/SQ
four	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S4/SQ
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S6/SR
seven	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D18/R2	D18/R2	X
eight	1	D19/R3	D19/R3	D20/R4	D20/R4	D21/R5	D21/R5	S8/SR
nine	1	D22/R6	D22/R6	D23/R7	D23/R7	D24/R8	D24/R8	S9/SP

Figure B-1.b Frame format of the intermediate data stream (8 kbit/s)
             with a synchronous user data rate of 2400 bit/s (V.110/X.30)

Extended data rate adaptor

OCTET	BIT NUMBER							
	one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1	D1	D1	D1	D2	D2	S1
two	1	D2	D2	D3	D3	D3	D3	X
three	1	D4	D4	D4	D4	D5	D5	S3
four	1	D5	D5	D6	D6	D6	D6	S4
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D7	D7	D7	D7	D8	D8	S6
seven	1	D8	D8	D9	D9	D9	D9	X
eight	1	D10	D10	D10	D10	D11	D11	S8
nine	1	D11	D11	D12	D12	D12	D12	S9

Figure B-1.c Frame format of the intermediate data stream (8 kbit/s) for a synchronous user data rate of 1200 bit/s (V.110).

Extended data rate adaptor   PCB2325

OCTET	one	two	three	four	five	six	seven	eight
			BIT NUMBER					
zero	0	0	0	0	0	0	0	0
one	1	D1 /P1	D1 /P1	D1 /P1	D1 /P1	D1 /P1	D1 /P1	S1/SP
two	1	D1 /P1	D1 /P1	D2 /P2	D2 /P2	D2 /P2	D2 /P2	X
three	1	D2 /P2	D2 /P2	D2 /P2	D2 /P2	D3 /P3	D3 /P3	S3/SP
four	1	D3 /P3	D3 /P3	D3 /P3	D3 /P3	D3 /P3	D3 /P3	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D4 /P4	D4 /P4	D4 /P4	D4 /P4	D4 /P4	D4 /P4	S6/SP
seven	1	D4 /P4	D4 /P4	D5 /P5	D5 /P5	D5 /P5	D5 /P5	X
eight	1	D5 /P5	D5 /P5	D5 /P5	D5 /P5	D6 /P6	D6 /P6	S8/SP
nine	1	D6 /P6	D6 /P6	D6 /P6	D6 /P6	D6 /P6	D6 /P6	S9/SP
zero	0	0	0	0	0	0	0	0
one	1	D7 /P7	D7 /P7	D7 /P7	D7 /P7	D7 /P7	D7 /P7	S1/SP
two	1	D7 /P7	D7 /P7	D8 /P8	D8 /P8	D8 /P8	D8 /P8	X
three	1	D8 /P8	D8 /P8	D8 /P8	D8 /P8	D9 /Q1	D9 /Q1	S3/SP
four	1	D9 /Q1	D9 /Q1	D9 /Q1	D9 /Q1	D9 /Q1	D9 /Q1	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	D10/Q2	S6/SQ
seven	1	D10/Q2	D10/Q2	D11/Q3	D11/Q3	D11/Q3	D11/Q3	X
eight	1	D11/Q3	D11/Q3	D11/Q3	D11/Q3	D12/Q4	D12/Q4	S8/SQ
nine	1	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	D12/Q4	S9/SP
zero	0	0	0	0	0	0	0	0
one	1	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	D13/Q5	S1/SP
two	1	D13/Q5	D13/Q5	D14/Q6	D14/Q6	D14/Q6	D14/Q6	X
three	1	D14/Q6	D14/Q6	D14/Q6	D14/Q6	D15/Q7	D15/Q7	S3/SP
four	1	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	D15/Q7	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	D16/Q8	S6/SP
seven	1	D16/Q8	D16/Q8	D17/R1	D17/R1	D17/R1	D17/R1	X
eight	1	D17/R1	D17/R1	D17/R1	D17/R1	D18/R2	D18/R2	S8/SP
nine	1	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	D18/R2	S9/SP
zero	0	0	0	0	0	0	0	0
one	1	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	D19/R3	S1/SP
two	1	D19/R3	D19/R3	D20/R4	D20/R4	D20/R4	D20/R4	X
three	1	D20/R4	D20/R4	D20/R4	D20/R4	D21/R5	D21/R5	S3/SP
four	1	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	D21/R5	S4/SP
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	D22/R6	S6/SP
seven	1	D22/R6	D22/R6	D23/R7	D23/R7	D23/R7	D23/R7	X
eight	1	D23/R7	D23/R7	D23/R7	D23/R7	D24/R8	D24/R8	S8/SP
nine	1	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	D24/R8	S9/SP

Figure B-1.d Frame format of the intermediate datastream (8 kbit/s) for the
user data rate speeds of 600 bit/s (V.110/X.30)

Extended data rate adaptor   PCB2325

OCTET	BIT NUMBER							
	one	two	three	four	five	six	seven	eight
one	1	D1 /P1	D2 /P2	D3 /P3	D4 /P4	D5 /P5	D6 /P6	S1/SQ
two	0	D7 /P7	D8 /P8	D9 /Q1	D10/Q2	D11/Q3	D12/Q4	X
three	1	D13/Q5	D14/Q6	D15/Q7	D16/Q8	D17/R1	D18/R2	S3/SR
four	1	D19/R3	D20/R4	D21/R5	D22/R6	D23/R7	D24/R8	S4/SP

Figure B-2 Frame format on the terminal highway for synchronous user data of
48 kbit/s and asynchronous user data upto 19.2 kbit/s (V-series
only).

OCTET	BIT NUMBER							
	one	two	three	four	five	six	seven	eight
one	D1	D2	D3	D4	D5	D6	D7	S
two	D8	D9	D10	D11	D12	D13	D14	S
three	D15	D16	D17	D18	D19	D20	D21	S
four	D22	D23	D24	D25	D26	D27	D28	S

Figure B-3 Frame format on the terminal highway for synchronous speed 56
kbit/s. When S is set '1', the framing fits to rec. V.110.

OCTET	BIT NUMBER							
	one	two	three	four	five	six	seven	eight
one	D1	D2	D3	D4	D5	D6	D7	D8
two	D9	D10	D11	D12	D13	D14	D15	D16
three	D17	D18	D19	D20	D21	D22	D23	D24
four	D25	D26	D27	D28	D29	D30	D31	D32

Figure B-4 Frame format on the terminal highway for synchronous speed of 64
kbit/s.

Extended data rate adaptor

PCB2325

Appendix C multiple sampling method
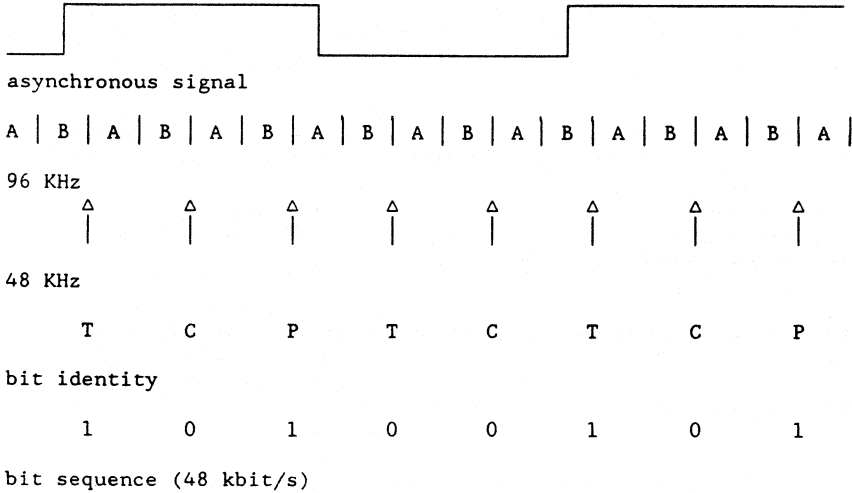
asynchronous signal

A | B | A | B | A | B | A | B | A | B | A | B | A | B | A | B | A |

96 KHz

48 KHz

    T   C   P   T   C   T   C   P

bit identity

    1   0   1   0   0   1   0   1

bit sequence (48 kbit/s)

code character for a transition (C)				position of the transition in a group of two sampling pulses
from 1 → 0		from 0 → 1		
T	C	T	C	
0	0	1	1	in first half (A)
0	1	1	0	in second half (B)

Figure C-5 Additional transition coding (based on R.111).

Additional transition coding is based on R.111. In R.111 however two transition code characters (C1 and C2) are used for each signal transition instead of one (C).

Extended data rate adaptor   PCB2325

Appendix D connection of the interchange circuits at 1200/75 bit/s

1200/75 mode   75/1200 mode

```
   DTE             EDRA               DTE          EDRA
 ────────  1200  ────────-         ──────── 75  ────────
   103 ─────────────▷ 103(EDRA-transmit 1200)   118 ───────────▷ 103
   105 ─────────────▷ 105              119  x
   106 ◁─────────── 106              120 ───────────▷ 105
   107 ◁─────────── 107              121 ◁─────────── 106
   108 ─────────────▷ 108              122  x

   118  x  75                         104 ◁─────────── 104
   119 ◁──────── 104(EDRA-receive 75)  107 ◁─────────── 107
   120  x                             108 ───────────▷ 108
   121  x                             109 ◁─────────── 109
   122 ◁──────── 109
```
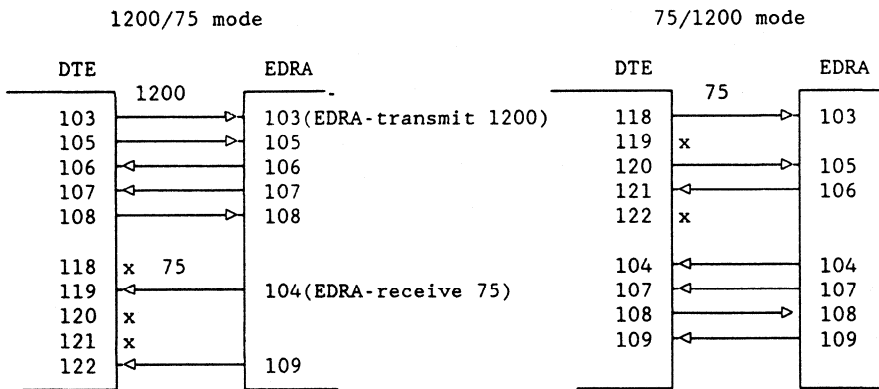
Figure D-1 Split speed (1200/75).

For the signal names of figure D-1 is referred to CCITT rec. V23.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

1. GENERAL DESCRIPTION

The 93C110 is a highly integrated 16/32-bit MICROCONTROLLER for use in a large variety of applications and is fully software compatible with the 68000. Integrating standard as well as advanced peripheral functions on the 93C110 (housed in an 84-pin package) dramatically reduces the system cost.

This document gives an overview of the basic functions, internal structure, and d.c. and a.c. characteristics. For further details about the features and operation of the 93C110 refer to "User manual SCC68070" (Hardware and Software).

The 93C110 has on-chip ROM, RAM and EEPROM. 34 KBytes of ROM are available for data, instructions and the interrupt vector table. The Random Access Memory composes 512 bytes of RAM and 256 bytes of Electrically Erasable Programmable ROM.

A total of 40 Input/Output pins are made available featuring standard or quasi-bidirectional features. An interrupt can be generated on changing states.

Extension for both peripheral units and memory up to 2 MBytes is made using dedicated 8051 and 68000 compatible buses.

Stand-by mode is available with a reduced supply current at low frequency.

The internal architecture of the 93C110 is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The 93C110 includes powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a 15 MHz clock signal for CPU and peripheral interfaces. The I^2C-bus interface allows easy and low-cost addition of peripherals (master and slave devices). The 93C110 also includes a UART interface. A built-in timer/counter with two independently programmable MATCH/COUNT/CAPTURE registers means that the 93C110 can be programmed with two of the following options simultaneously:

* pulse generator
* external event counter
* reference timer
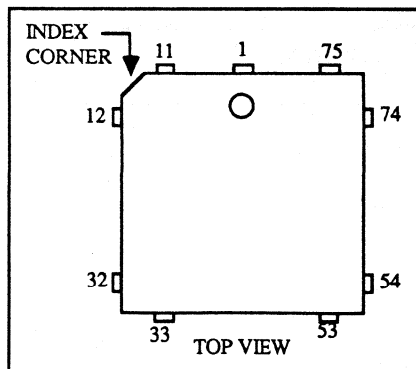
Fig.1 PIN CONFIGURATION

1.1 FEATURES

- CHMOS technology
- 32-bit internal structure
- Maximum internal clock frequency: 15 MHz
- 84-pin package
- 8 programmable interrupt inputs
- On-chip   ROM   34 KBytes
                  RAM   512 Bytes
                  EEPROM 256 Bytes
- Built-in clock generator:
                  max. 30 MHz crystal
- Reset control circuitry
- On-chip address decoder
- 16-bit input/output General Purpose Port
- 8-bit input/output Auxiliary Port
- 16-bit input/output Secondary Port
- I2C serial bus interface
- UART serial interface
- 16-bit timer/counter
- Two 16-bit match/count/capture registers
- Full 68000 software compatibility
- 68000-compatible bus interface (15 MHz)
- 56 powerful instruction types
- 5 basic data types
- 2 MByte addressing range
- 14 addressing modes
- Memory-mapped I/O
- Autovectored interrupts
- 7 interrupt levels
- Stand-by modes
- 80C51 bus interface compatible

1.2 ORDERING INFORMATION

TYPE NUMBERS	TEMPERATURE RANGE	PACKAGE
PCB 93C110	0 to 70°C	84-pin PLCC
PCF 93C110	-40 to 85°C	84-pin PLCC

1.3 BLOCK DIAGRAM
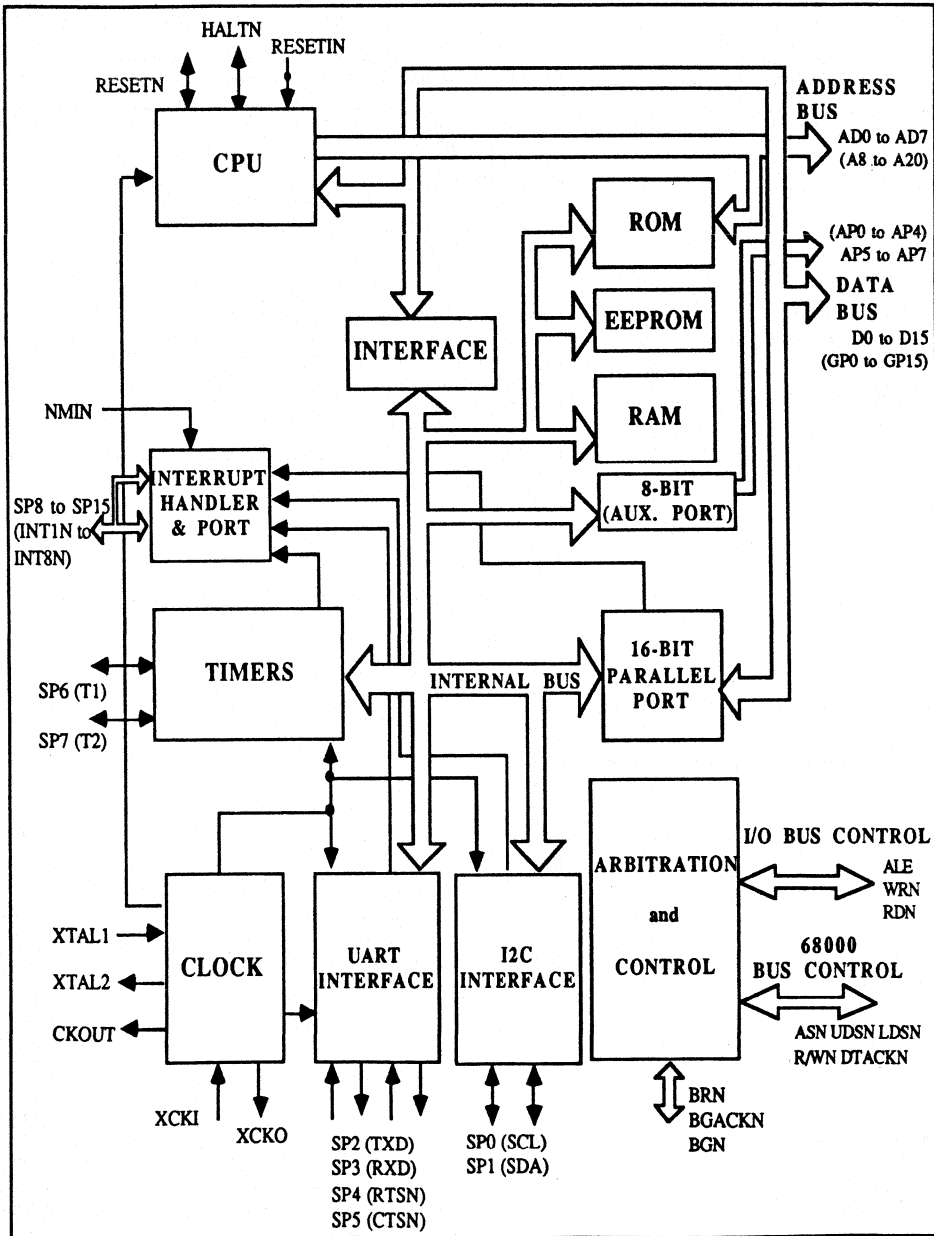
Fig.2 BLOCK DIAGRAM

2. SIGNAL DESCRIPTION

Pu: Pin with high impedance pull-up resistor

MNEMONIC	TYPE	PIN NO.	FUNCTION
AD0 to AD7	O		(Active-HIGH, tri-state)Address/Data - multiplexed bus for peripheral extension (8051), used as LSBs for address bus during memory extension cycles (68K).
A8 to A15	O		(Active-HIGH, tri-state) Address - lines used as MSBs for peripheral extension cycles and has middle part of address bus for memory extension cycles.
AP0 to AP4 (A16 to A20) (PCS0 to PCS3)	I/O		Auxiliary I/O port. Alternate functions can be either the MSBs of address in Memory extension cycles or Chip selects.
GP0 to GP15 (D0 to D15)	I/O		(Active-HIGH, tri-state) General Purpose Port. Alternate function 16-bit Data bus bidirectional for the 68K memory.
ASN	O		(Active-LOW, tri-state) Address Strobe - indicates a valid address on the bus.
LDSN	O		(Active-LOW, tri-state) Lower Data Strobe - indicates that: - For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). - For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O		(Active-LOW, tri-state) Upper Data Strobe - indicates that: - For a WRITE cycle, the data is valid on the upper half of the data bus (D8 to D15). - For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O		Read (active-High)/Write (active-Low) - controls the direction of the data flow of the memory bus cycle.
DTACKN	I		(Active-LOW)Data Transfer Acknowledge - asserted by the peripheral during CPU bus cycles when data is either received from or placed on the bus. If not asserted punctually it causes the CPU to insert wait states.
BRN	I		(Active-LOW) Bus Request - asserted by wire-ORed external DMA devices that request bus ownership.
BGN	O		(Active-LOW, Open drain) Bus Grant Output - a daisy chain output which is asserted by the 93C110 when the bus is granted by the CPU.
BGACKN	I/O		(Active-LOW, Open drain) Bus Grant Acknowledge - asserted by any external DMA device that has control of the bus or by the internal 80C51 bus control. As long as this line is held LOW externally, the 93C110 will hold the bus signals in high impedance state. When BGACKN is released, the 93C110 will have access to the bus. Note that interrupts cannot be serviced while BGACKN is held LOW.
RESETN	I/O		(Active-LOW, Open drain) Bidirectional Reset - if asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the Reset instruction resets external hardware or on-chip peripherals.

MNEMONIC	TYPE	PIN NO	FUNCTION
HALTN	I/O		(Active-LOW, Open drain) Bidirectional Halt - if asserted externally together with RESETN, it causes the 93C110 to enter the Reset state. If asserted alone, it will cause the CPU to stop after completion of the current bus cycle. As long as HALTN is held LOW, all control signals are inactive and all tri-state lines are placed in the high-impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault), the processor drives this line LOW.
NMIN	I		(Active-LOW) Non-Maskable Interrupt (level 7) - while the other interrupts may be masked (disabled), this interrupt is always enabled. The low level must be maintained until the interrupt acknowledge cycle is performed.
SP8 to SP15 (INT1N to INT8N)	I/O	Pu	(Active-LOW) Latched Interrupt Inputs - a LOW level of ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable. Also usable as Input/Output port.
RESETIN			(Active-HIGH) Reset Input Line - to be connected to an external capacitor in order to provide the correct reset sequence at power-up.
V_{DD}			Supply voltage +5.0 V nominal.
V_{SS}			Ground.
XTAL1 XTAL2	I		External Crystal Inputs - XTAL1 can be used as a clock-input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O		Clock Out - this is the reference from the internal system clock.
MODE 0, 1	I		Input lines defining the memory map to be used and the activation of the 16-bit parallel port or the 16-bit data bus.
ALE	O		Address Latch Enable Output - used to latch the low byte of address (AD0-AD7) during access to external 8051 bus compatible peripheral circuits.
WRN	O		(Active-LOW) External Peripheral Write Strobe.
RDN	O		(Active-LOW) External Peripheral Read Strobe.
CSROMN	O		(Active-LOW) ROM Chip Select - decodes a size of 512 KBytes mapped from 1.5 to 2 MBytes (available in the 4 modes). CSROMN is also asserted during the read cycles of the Reset Vector.
CSRAMN	O		(Active-LOW) RAM Chip Select - decodes a size of 512 KBytes mapped from 1 MB to 1.5 MBytes (available in the 4 modes).
AP5 to AP7	I/O		Auxiliary I/O Port (always available).

MNEMONIC	TYPE	PIN NO.	FUNCTION
SCL (SP0)	I/O		(Open drain) Serial Clock - SCL is the clock signal for the I2C-bus operation. It is either driven by the 93C110 when the I2C interface is in the master mode, or it is the clock input if the I2C interface is in the slave mode.
SDA (SP1)	I/O		(Open drain) Serial Data - SDA is the data signal for the I2C-bus.
T1 (SP6) T2 (SP7)	I/O		(Tri-state) Timers 1 & 2 - these are I/O signals for the capture timers of channels 1 & 2 respectively. They can be programmed as either outputs for pulses or inputs for for count cycles and events.
RXD (SP3)	I/O		Receive Data - RXD is the data input for the UART serial interface.
TXD (SP2)	I/O		Transmit Data - TXD is data output for the UART serial interface.
RTSN (SP4)	I/O		(Active-LOW) Request To Send - this output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN (SP5)	I/O		(Active-LOW) Clear To Send - this input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected to each other if no control lines are needed.
XCKI	I		External Clock - when selected, XCKI is the clock input for the UART serial interface. This signal can be used: - to generate special baud rates. - when a crystal frequency other than 29.491 MHz is used by the 93C110, an external clock of 9.8304 MHz can be connected to this input to generate the standard baud rates.
XCKO	I		Auxiliary Oscillator Output - to be connected (with XCKI) to a crystal to generate the auxiliary clock for the UART or the CPU. Can be used as a low-cost RC oscillator for stand-by function.
SP0 to SP7	I/O		May be used as input/output ports if the alternate function is not used.

Test Point	R_L (KΩ)	C_L (pF)
RESETN	1	130
HALTN	1	130
SDA	2	400
SCL	2	400
BGACKN	1	130

Fig.29 OPEN DRAIN,
BI-DIRECTIONAL TEST LOADS.

C_L = 130 pF (including all parasitics) except CKOUT for which C_L = 50 pF

V_{TH} = 1.6 V.system load threshold voltage at which dynamic loads (I_{OH} and I_{OL}) switch; see D.C. characteristics.

Fig.30 REMAINING TEST LOADS.

10.2 DC CHARACTERISTICS

V_{DD} = 5.0 V ±20%, V_{SS} = O V; T_{amb} = -40 to 85 ºC (see Figures 42 and 43)[4,5]

parameter	test conditions	LIMITS min.	max.	unit
V_{IH} Input voltage HIGH, all inputs except				
XTAL1, XTAL2, SDA, SCL, XCKI		2.0	V_{DD}	V
XTAL1, XCKI		0.8V_{DD}	V_{DD}	V
SDA, SCL		3.0	V_{DD}	V
V_{IL} Input voltage LOW, all inputs				
except SDA, SCL		VSS - 0.3	0.8	V
SDA, SCL		VSS - 0.3	1.5	V
I_{in} Input leakage current	V_{DD} = 5.25 V			
RSTN, CTSN, XCKI,BRN, DTACKN,INT1N to INT8N and XTAL1			20	µA

parameter	test conditions	LIMITS		unit
		min.	max.	
I_{TSI} Tri-state (off-state) input current A1-A23, D0-D15, ASN, LDSN, R/WN, UDSN, T1, and T2	V_{in} = 2.4/0.4 V		20	μA
I_{ODI} Open-drain (off-state) input current BGACKN, RESETN, HALTN, SCL and SDA			20	μA
V_{OH} Output voltage HIGH CKOUT	I_{OH} = 400 μA	$0.8V_{DD}$		V
A1-A23, D0-D15, ASN, BGN, LDSN, R/WN, UDSN, T1, T2, TXD, CSROMN and CSRAMN		2.4		V
V_{OL} Output voltage LOW HALTN, A1-A23, BGN, BGACKN, RESETN, T1, T2, TXD, RTSN, ASN, D0-D15, LDSN, R/WN and UDSN	I_{OL} = 3.2 mA		0.5	V
CKOUT, CSROMN and CSRAMN	I_{OL} = 3.2 mA		0.45	V
SDA and SCL	I_{OL} = 5.0 mA	0.45		V
I_{DD} Current Consumption	CKOUT freq. = 15 MHz		t.b.f.	mA
C_{in} Capacitance	V_{in} = OV, T_{amb} = 25ºC frequency = 1 MHz		20	pF
I_{id} Current consumption in Idle mode	CKOUT f = 15 MHz XCKI f = 300 kHz		20	mA
I_{stby} Current consumption in Stand-by mode	XCKI f = 300 kHz		t.b.f.	mA
I_{stop} Current consumption in Stop mode	XCKI f = 300 kHz		t.b.f.	mA

10.3 AC CHARACTERISTICS

Crystal frequency = 30 MHz, V_{DD} = 5 V ±20%, V_{SS} = 0 V, T_{amb} = -40 to =85ºC, C_{load} on CKOUT = 50 pF (see figs.31 to 34).

<div style="writing-mode: vertical">OBJECTIVE SPECIFICATION</div>

number	parameter	symbol	TENTATIVE LIMITS min.	max.	unit
1	CRYSTAL or INPUT (XTAL1) clock period		33	125	ns
1A	XTAL high to CKOUT high or low		5	40	ns
2	CKOUT low level		20		ns
3	CKOUT high level		20		ns
4	CKOUT fall time			10	ns
5	CKOUT rise time			10	ns
6	CKOUT low to address valid			50	ns
7	CKOUT high to address/data high imp.			55	ns
8	CKOUT high to address invalid (min.)		0		ns
9	CKOUT high to ASN, DSN low		0	45	ns
11	Address to ASN/DSN low		10		ns
12	CKOUT low to ASN, DSN high		0	45	ns
13	ASN, DSN high to address invalid		10		ns
14	ASN/DSN (read), ASN (write) low level		130		ns
14A	DSN low level (write)		65		ns
15	ASN, DSN high level		70		ns
16	CKOUT high to ASN, DSN high impedance			50	ns
17	ASN, DSN high to RWN high (read)		10		ns
18	CKOUT high to RWN high		0	45	ns
20	CKOUT high to RWN low (write)			45	ns
21	Address valid to RWN low (write)		0		ns
22	RWN low to DSN low (write)		25		ns
23	CKOUT low to data-out valid (write)			45	ns
25	ASN, DSN high to data-out invalid		15		ns
26	Data-out valid to DSN low (write)		15		ns
27	Data-in to clock low (set-up time, read)		5		ns
28	ASN, DSN high to DTACKN, RDYN, AVN high		0	120	ns
29	ASN, DSN high to data invalid (hold time)		0		ns
30	ASN, DSN high to BERRN high		0		ns
31	DTACKN low to data-in (set-up time, read)		45	ns	
32	HALTN and RESETN input transition time		0	200	ns
33	CKOUT high to BGN low			50	ns
34	CKOUT high to BGN high			50	ns
35	BRN low to BGN low		1.5	3.5 +70	cp ns
36	BRN high to BGN high		1.5	2.5 +70	cp ns
37	BGACKN low to BGN high		1.5	2.5 +70	cp ns
38	BGN low to bus high impedance			50	ns
39	BGN high level		1.5		cp
40	BGACKN width		1.5		cp
41	Asynchronous input set-up time		25		ns
41A	Asynchronous input set-up time (DTACKN)		10		ns
43	CKOUT high to data-out invalid (write)		0		ns
44	RWN low to data bus driven		10		ns
45	HALTN/RESETN pulse width		10		cp
46	CKOUT LOW to BRN LOW (see note 2)			40	ns
47	CKOUT HIGH to BGACKN (output) LOW			60	ns

10.4 PERIPHERAL BUS INTERFACE

number	parameter	symbol	Variable CKOUT clock min.	max.	unit
1	Oscillator frequency	1/TCLCL		30	MHz
49	CKOUT Clock frequency	1/TCKOU		15	MHz
50	ALE pulse width	TLHLL	2TCKOU-40		ns
51	Address valid to ALE low	TAVLL	1/2TCKOU-22		ns
52	Address hold after ALE low	TLLAX	TCKOU-35		ns
53	RD pulse width	TRLRH	5TCKOU-33		ns
54	WR pulse width	TWLWH	5TCKOU-33		ns
55	RD low to valid data-in	TRLDV		4.5TCKOU-132	ns
56	Data hold after RD	TRHDX	0		ns
57	Data float after RD	TRHDZ		0.5TCKOU	ns
58	ALE low to valid data-in	TLLDV		7.5TCKOU-117	ns
59	Address to valid data-in	TAVDV		8TCKOU-98	ns
60	ALE low RD or WR low	TLLWL	3TCKOU-50	3TCKOU+50	ns
61	Address valid to Write low	TAVWL	3.5TCKOU-96		ns
62	Data valid to WRn transition	TQVWX	2TCKOU-70		ns
63	Data valid to WRn high	TQVWH	7TCKOU-103		ns
64	Data hold after WRn	TWHQX	1TCKOU-50		ns
65	RDn low to address float	TRALZ	0		ns
66	RDn or WRn high to ALE high	TWHLH	TCKOU-40	TCKOU+40	ns

10.5 POWER CONSIDERATIONS

The average chip-junction temperature, T_j, in °C can be obtained from:

$$T_j = T_{amb} + (P_D \times R_{THJA}) \tag{1}$$

where:

T_{amb} = ambient temperature, °C.

R_{THJA} = package thermal resistance, junction-to-ambient, °C/W.

$$P_D = P_{INT} + P_{I/0} \tag{2}$$

P_{INT} = $I_{DD} \times V_{DD}$ = chip internal power W.

$P_{I/0}$ = power dissipation on input and output pins (determined by the user).

For most applications $P_{I/0} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_j (if $P_{I/0}$ is neglected) is:

$$P_D = K + (T_j + 273).$$

Solving equations (1) and (2) for K gives:

$$K = P_O(T_{amb} + 273) + R_{THJA}P_D^2 \tag{3}$$

Where K is a constant pertaining to a particular part, K can be determined from equation (3) by measuring P (at equilibrium) for a known T_{amb}. Using this value of K, the values of P_D and T_j can be obtained by solving equations (1) and (2) iteratively for any value of T_{amb}.

DEVELOPMENT DATA

This data sheet contains advance information and
specifications are subject to change without notice.

PCF2322

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

WIDEBAND SPEECH ENCODER/DECODER

GENERAL DESCRIPTION

The PCF2322 is a high quality speech encoder/decoder that produces a bit-for-bit compatible solution
with the CCITT G.722 standard. The G.722 coding system allows the transmission of a 50 Hz to 7 kHz
audio signal within a bit rate of 64 kbit/s (8 bits per time slot, repeated at an 8 kHz rate). The system
uses sub-band adaptive differential pulse code modulation (SB ADPCM) that can be driven in three
different modes of operation.

The 7 kHz audio signal can be transmitted within rates of 64, 56 or 48 kbit/s. The other two modes
allow an auxiliary data channel of 8 and 16 kbit/s respectively.

Features

- Sub-band Adaptive Differential Pulse Code Modulation (SB ADPCM)
- Compatible with CCITT G.722 standard
- Three operational modes
- 50 Hz to 7 kHz audio bandwidth
- Test sequences compatible with CCITT

ORDERING INFORMATION

type number	package	maximum clock frequency (MHz)	temperature range
PCF2322WP	PLCC68	8.2	−40 to + 85 °C

PACKAGE OUTLINE

68-lead PLCC; (SOT188AA, AGA)
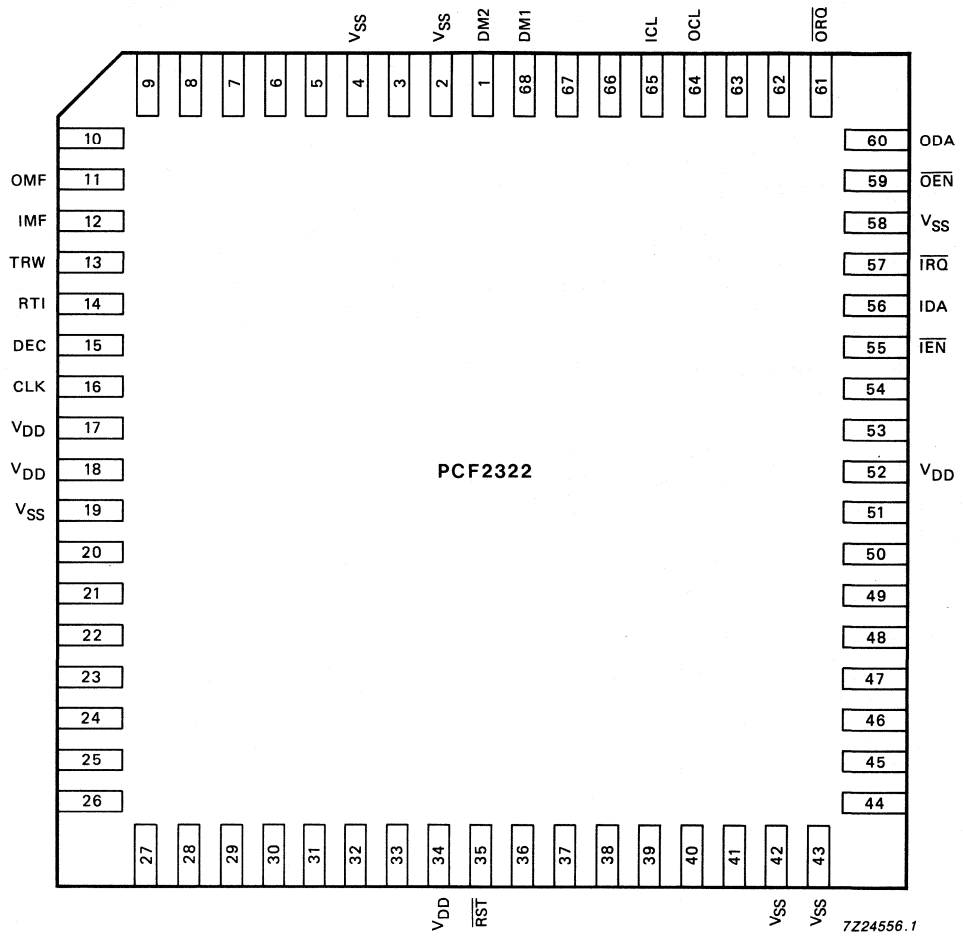
Fig.1 Pinning diagram.

* All pins not designated should not be connected.

FUNCTIONAL DESCRIPTION

The PCF2322 produces a bit-for-bit compatible solution with the CCITT test sequence. With one PCF2322 a half duplex transcoder is accomplished which can provide capability as either an encoder or a decoder.

Table 1 Signal description

signal	I/O	description
V_{DD}	I	supply voltage: 5 V ± 5%
V_{SS}	–	ground
CLK	I	master clock
$\overline{RST}$	I	reset
DEC	I	decoder/encoder
RTI	I	real-time test
TRW	I	14 bit/16 bit
IMF	I	input MSB first/LSB first
OMF	I	output MSB first/LSB first
DM1	I	decoder mode 1
DM2	I	decoder mode 2
IDA	I	input data
$\overline{IEN}$	I	input enable
$\overline{IRQ}$	O	input request
ICL	I	input clock
ODA	O	output data
$\overline{OEN}$	I	output enable
$\overline{ORQ}$	O	output request
OCL	I	output clock

DEVELOPMENT DATA

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	6.5	V
Total power dissipation		P_{tot}	−	1	W
Voltage at any input		V_I	−0.5	$V_{DD} + 0.5$	V
Output current		I_O	−	5	mA
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

DC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = −40 to + 85 °C; all voltages are measured with respect to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage		V_{DD}	4.75	−	5.25	V
Supply current	notes 1 and 2	I_{DD}	−	100	130	mA
HIGH level input voltage	except CLK	V_{IH}	2.0	−	$V_{DD} + 0.5$	V
HIGH level input voltage	CLK only	V_{IH1}	2.4	−	$V_{DD} + 0.5$	V
LOW level input voltage		V_{IL}	−0.5	−	+ 0.8	V
LOW level input current	V_I = 0.4 V	$-I_{IL}$	−	−	100	μA
HIGH level input current	V_I = 2.0 V	$-I_{IH}$	−	−	100	μA
HIGH level output voltage	$-I_{OH}$ = 100 μA	V_{OH}	2.4	−	−	V
LOW level output voltage	I_{OL} = 2 mA	V_{OL}	−	−	0.4	V

Notes to the DC characteristics

1. I_{DD} (typ.) is based on V_{DD} = 5 V; T_{amb} = 22 °C under operating conditions (excluding the reset condition).

2. $I_{DD(max.)}$ is based on V_{DD} = $V_{DD(max.)}$, $\overline{RST}$ = 0, f = 8.2 MHz and all other pins disconnected.

AC CHARACTERISTICS

V_{DD} = 5 V ± 5%; T_{amb} = −40 to +85 °C; C_L = 80 pF (capacitive load per output); I_{OL} = 2 mA; −I_{OH} = 100 μA; timing measurements are taken at 2 V for logic 1 and 0.8 V for logic 0; all voltages are measured with respect to ground; unless otherwise specified

no.*	parameter	min.	max.	unit
1	CLK rise time; ICL and OCL	—	6	ns
2	CLK fall time; ICL and OCL	—	6	ns
3	CLK period	122	2000	ns
4	CLK width HIGH	55	1000	ns
5	CLK width LOW	55	1000	ns
6	ICL and OCL period	244	—	ns
7	ICL and OCL width HIGH	110	—	ns
8	ICL and OCL width LOW	110	—	ns
9	$\overline{RST}$ set-up time	10	—	ns
10	$\overline{RST}$ hold time	30	—	ns
11	ICL LOW to $\overline{IRQ}$ LOW	—	40	ns
12	ICL LOW to IRQ HIGH	—	40	ns
13	$\overline{IEN}$ set-up time	30	—	ns
14	IEN hold time	10	—	ns
15	IDA set-up time	10	—	ns
16	IDA hold time	40	—	ns
17	OCL LOW to $\overline{ORQ}$ LOW	—	40	ns
18	OCL LOW to $\overline{ORQ}$ HIGH	—	40	ns
19	$\overline{OEN}$ set-up time	40	—	ns
20	OEN hold time	10	—	ns
21	OCL LOW to next ODA valid	—	40	ns
22	$\overline{OEN}$ LOW to ODA valid	—	40	ns
23	$\overline{OEN}$ HIGH to ODA 3-state	—	40	ns

DEVELOPMENT DATA

* Numbers cross-refer to Figs 2, 3, 4 and 5.

Data sheet	
status	Preliminary specification
date of issue	March 1991

PCF5012
14-bit ADC/DAC converter

GENERAL DESCRIPTION

The PCF5012 is an integrated circuit which implements a full 14-bit analog-to-digital and digital-to-analog conversion system. It includes all band-limiting filters. The analog-to-digital and digital-to-analog converters operate according to the one-bit interpolative conversion principle, whereby quantization noise shaping is used.

The PCF5012 is optimized for use in combination with a digital signal processor. Telecom terminals is one of the application areas.

FEATURES

- Complete analog-to-digital and digital-to-analog 14-bit conversion system
- Implemented using Philips 'Bit Stream' techniques
- Suitable for use in G.722 wideband speech CODECs
- No external sample-and-hold, simple/no analog pre and post filtering required: all filters are digitally integrated
- No need for internal trimming, no performance degradation
- Very high linearity
- Sampling rate in the range of 8 kHz to 16 kHz
- High bandwidth of the analog signal: 7 kHz (f_s = 16 kHz)
- Needs only a few external components
- Easily connectable to a DSP via a serial or parallel interface
- Low power consumption

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF5012P	28	DIL28	plastic	SOT117
PCF5012H	44	QFP44	plastic	SOT205A
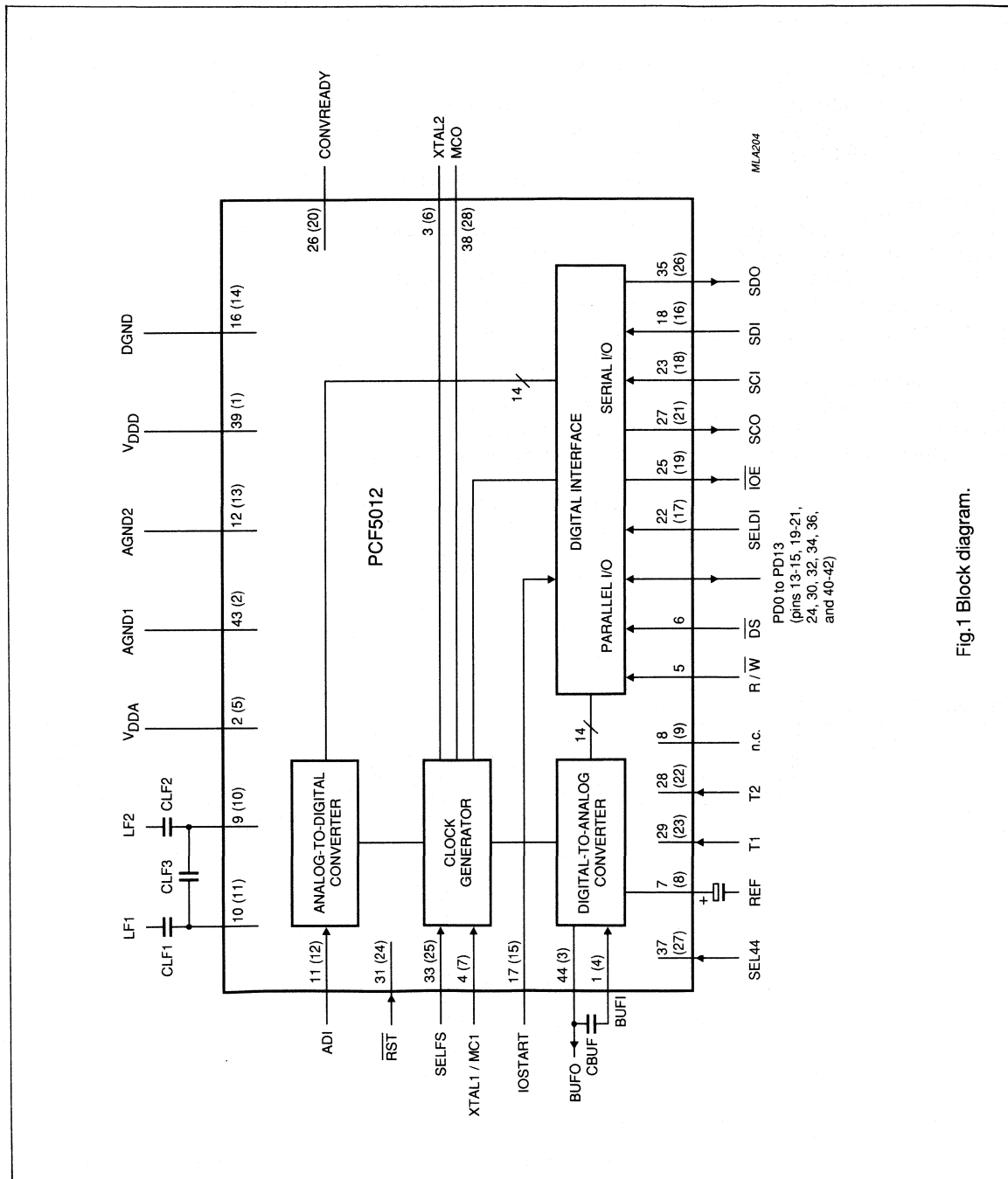
Fig.1 Block diagram.

MLA204

14-bit ADC/DAC converter
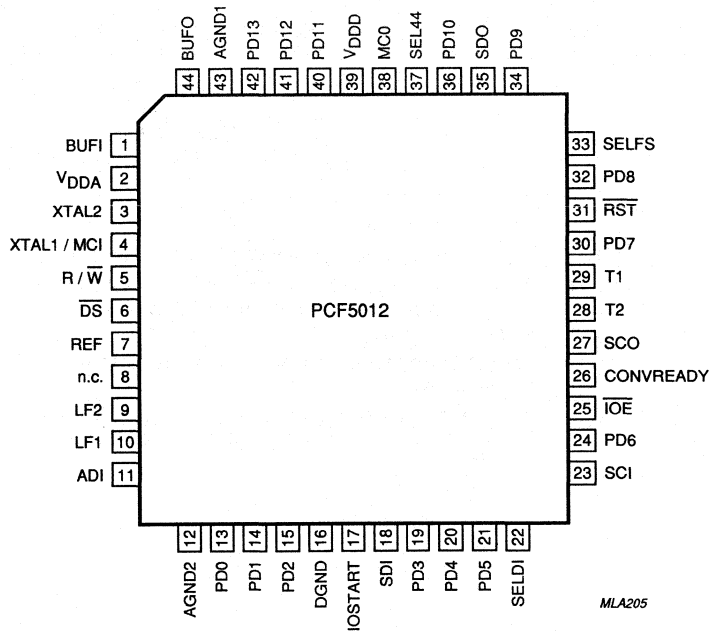
PCF5012

Fig.2(a) Pin configuration (QFP44).
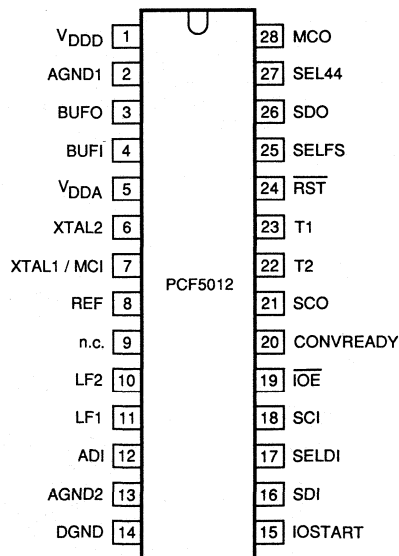
Fig.2(b) Pin configuration (DIL28).

14-bit ADC/DAC converter

PCF5012

PINNING

The pin numbers without brackets refer to the QFP44 package and the pin numbers between brackets refer to the DIL28 package.

SYMBOL	PIN	DESCRIPTION
BUFI	1 (4)	DAC buffer input. Used for external filter capacitor from BUFO
V_{DDA}	2 (5)	analog supply voltage connected to V_{DDD}
XTAL2	3 (6)	crystal connection
XTAL1/MC1	4 (7)	crystal connection or external system clock input
R/$\overline{W}$	5	defines the direction of the data transfer across the parallel interface.When R/$\overline{W}$ = HIGH processor reads from PCF5012. When R/$\overline{W}$ = LOW processor writes to PCF5012
$\overline{DS}$	6	data strobe signal to activate the data transfer across the parallel interface (active LOW)
REF	7 (8)	the reference for all internal analog signals is derived from the analog supply. Therefore a capacitor for external reference filtering should be connected to the REF pin
n.c.	8 (9)	not connected
LF2	9 (10)	external capacitor for ADC loop filter
LF1	10 (11)	external capacitor for ADC loop filter
ADI	11 (12)	analog signal input referenced to REF
AGND2	12 (13)	analog ground connected to DGND
PD0	13	bidirectional parallel data line, LSB
PD1	14	bidirectional parallel data line
PD2	15	bidirectional parallel data line
DGND	16 (14)	digital ground
IOSTART	17 (15)	LOW-to-HIGH transition starts the I/O transfer. After a LOW-to-HIGH transition of CONVREADY the serial I/O can be started with IOSTART. This can be achieved externally or by connection to CONVREADY (Master PCF5012). If several PCF5012s share a common multiplexed serial port they can be synchronized by connecting $\overline{IOE}$ to IOSTART of the next (Slave PCF5012) in cascade
SDI	18 (16)	serial data input. Data shifted in MSB-first with rising edge of SCI
PD3	19	bidirectional parallel data line
PD4	20	bidirectional parallel data line
PD5	21	bidirectional parallel data line
SELDI	22 (17)	selects between serial (SELDI = HIGH) or parallel (SELDI = LOW) interface
SCI	23 (18)	shift clock supply for the serial interface
PD6	24	bidirectional parallel data line
$\overline{IOE}$	25 (19)	input/output data transfer via the digital interfaces, starts when LOW
CONVREADY	26 (20)	clock with the frequency f_s. A LOW-to-HIGH transition indicates that the PCF5012 is ready for a new I/O procedure. This signal can be used to synchronize the whole system
SCO	27 (21)	buffered internal clock (128 x f_s) for the serial data interface in the "stand alone" operation. (independent of $\overline{RST}$)
T2	28 (22)	test pin. Has to be connected to V_{DDD}
T1	29 (23)	test pin. Has to be connected to V_{DDD}

14-bit ADC/DAC converter

PCF5012

SYMBOL	PIN	DESCRIPTION
PD7	30	bidirectional parallel data line
$\overline{\text{RST}}$	31 (24)	reset signal. The internal sequencer starts at a defined position. Digital interfaces are muted for a time of $32/f_s$
PD8	32	bidirectional parallel data line
SELFS	33 (25)	selects the ratio of f_s and the system clock. SELFS = HIGH; f_s = MCO/1024 SELFS = LOW; f_s = MCO/512
PD9	34	bidirectional parallel data line
SDO	35 (26)	serial data output 3-state. Data shifted out MSB first with falling edge of SCI
PD10	36	bidirectional parallel data line
SEL44	37 (27)	has to be connected HIGH for 44-pin package; LOW for 28-pin package
MCO	38 (28)	buffered system clock output from MCI (independent from $\overline{\text{RST}}$)
V_{DDD}	39 (1)	digital supply voltage (+5 V)
PD11	40	bidirectional parallel data line
PD12	41	bidirectional parallel data line
PD13	42	bidirectional parallel data line, MSB
AGND1	43 (2)	analog ground connected to DGND
BUF0	44 (3)	buffer for analog output. Output is referenced to REF

Note to the pinning

All SELect inputs are meant to be 'static' inputs to configure the system and can cause corruption of the system when they are switched during operation.

14-bit ADC/DAC converter

PCF5012

FUNCTIONAL DESCRIPTION

Figure 1 shows the functional block diagram of the PCF5012.
The analog-to-digital and digital-to-analog converter, the digital interfaces and the clock generator are described separately in the subsequent sections.

Analog-to-digital converter (ADC)

The ADC consists of an analog input block which produces a 1-bit code, by means of oversampling ($128 \times f_s$) and noise shaping, and a digital decimation filter, which converts the 1-bit code into a 14-bit signal and reduces the sampling rate to f_s. The 14-bit code is then transmitted via the digital interfaces.
It is possible to vary the sampling rate f_s between 8 and 16 kHz by varying the system clock rate or the clock divider (SELFS).

Three external capacitors are required for the loop filter:

$CLF1 = 220$ pF $\times$ 16 kHz/f_s,
$CLF2 = 330$ pF $\times$ 16 kHz/f_s and
$CLF3 = CLF2/10.7$

Digital-to-analog converter (DAC)

The DAC consists of a digital interpolation filter, a noise shaping coder, a 1-bit DAC and a buffer amplifier.
The interpolation filter increases the sampling rate of the digital input signal and suppresses periodic spectral signal components within the audible range.

The noise shaping coder reduces the word length to 1 bit and feeds back the resulting quantization noise (noise shaping). This noise spectrum rises with 12 dB/octave above the audible range. A first order filter can

be included in the DAC by connecting one external capacitor (CBUF) between BUFI and BUFO (CBUF = 150 nF $\times$ 16 kHz/f_s). This filter is adequate for applications in which the ear is the receiver. For more critical applications, in which the DAC signal is resampled or mixed, further post-filtering of at least first order should be provided.

Digital interfaces

The PCF5012 has separate serial input and output ports. The data is transferred simultaneously on both serial ports. In the 44-pin version a parallel data exchange is provided for a 14-bit wide bidirectional parallel data interface. SELDI (Select Data Interface) determines whether the parallel or the serial interface is used.

The digital interfaces are arranged such that the PCF5012 can be directly connected to a signal processor (PCB5010/11) without the need for additional external "glue" logic. The number format is in two's complement notation.

Serial Interfaces

Digital data transfer to and from the PCF5012 can take place via the serial I/O interfaces. The interface consists of two data lines SDI and SDO (Serial Data In and Serial Data Out) and two clock lines SCI and SCO (Serial Clock In and Serial Clock Out). The serial clock input (SCI) is common to both serial interfaces and must be supplied by the system.
For stand alone applications, SCI can be connected to the SCO output which supplies a buffered internal clock ($128 \times f_s$). The maximum transfer rate is 4 Mbits/s.

The PCF5012 writes 14-bits serial data, on the falling edge of SCI, to the data output SDO and reads 14-bits serial data, on the rising edge of SCI, from the data input SDI. The MSB of a PCM word is transferred in the first bit position, which is compatible to most converters and nearly compatible to the I²S-Interface.

The serial I/O operation can be started after a LOW-to-HIGH transition of CONVREADY. It is triggered by a LOW-to-HIGH transition on the IOSTART pin which is detected at the LOW-to-HIGH transition of SCI. IOSTART can be used to trigger the I/O either externally or internally by connecting it to CONVREADY. During the serial data transfer the $\overline{IOE}$ pin is held LOW for fourteen SCI cycles. The I/O operation has to be completed three SCO cycles before the next LOW-to-HIGH transition of CONVREADY to prevent data collision with the internal data exchange.
Should $\overline{IOE}$ become non-active (HIGH) then the output SDO will go to the 3-state condition and the input SDI will be inhibited. This allows the possibility to multiplex several serial I/Os onto a common serial port of a signal processor. In this situation, the arbitration of several serial interfaces has to be solved.

One simple solution is to connect the $\overline{IOE}$ output of one PCF5012 to the IOSTART input of the next PCF5012. In this way a cascade of PCF5012s can be built so that the end of a transfer on one PCF5012 starts the begining of the transfer of the next PCF5012. The first PCF5012 can be configured as a master, (IOSTART = CONVREADY) or, started by an external trigger being applied to its IOSTART input.

14-bit ADC/DAC converter
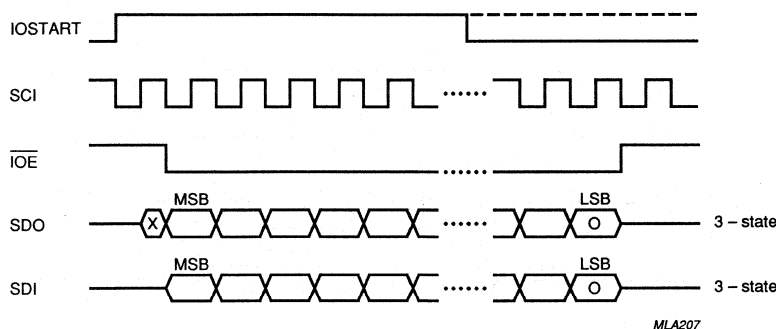
PCF5012

Fig.3 Functional timing diagram for the serial data transfer.

Parallel Interface

(44-pin package only)

The parallel interface can be used instead of the serial interfaces for the digital transfer to and from the PCF5012. The connections are bidirectional and do not need additional external "glue" logic.

The interface consists of the parallel data lines PD0 (LSB) to PD13 (MSB) and the control inputs R/$\overline{W}$ and $\overline{DS}$. After a LOW-to-HIGH transition of CONVREADY a parallel I/O operation can be started. It has to be completed three SCO cycles before the next LOW-to-HIGH transition of CONVREADY to prevent data collision with the internal data

exchange. During this period the transfer can take place completely asynchronously and is controlled from the processor via the R/$\overline{W}$ and $\overline{DS}$ control lines.

The R/$\overline{W}$ signal switches the direction of the parallel data transfer from WRITE to READ and vice-versa. When R/$\overline{W}$ = HIGH a READ operation from the PCF5012 to the processor is indicated, and when R/$\overline{W}$ = LOW a WRITE operation from the processor to the PCF5012 is indicated. The signal $\overline{DS}$ defines the time at which the data output is valid ($\overline{DS}$ = LOW), the data being accepted by the interface (LOW-to-HIGH transition of $\overline{DS}$). The 3-state buffers of the

parallel interface are in a 3-state condition when $\overline{DS}$ is inactive ($\overline{DS}$ = HIGH). This enables the PCF5012 to be memory mapped into the address areas of the processor.

By means of a control signal SELDI (Select Data Interface) the user can define which of the digital interfaces (serial or parallel) is to be used for actual data exchange to the PCF5012.

14-bit ADC/DAC converter
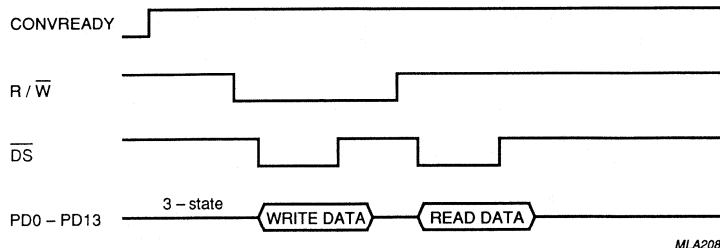
PCF5012

Fig.4 Functional timing diagram for the parallel data transfer.

Clock generator

The PCF5012 can generate a system clock by connecting a crystal to the crystal oscillator (XTAL1 and XTAL2). Alternatively, an external clock generator can also be connected to the XTAL1-MCI input.

Since the timing of the analog blocks is derived from this clock it must not contain any clock jitter. Any low frequency jitter, would modulate the analog signals and degrade the performance. The buffered master clock is available at the MCO output.

The PCF5012 derives the sampling rate, f_s, by dividing the master clock. The SELFS input can be used to set the division ratio either to 1024 (SELFS = HIGH) or to 512 (SELFS = LOW).

Reset (via $\overline{RST}$ pin)

A Reset ($\overline{RST}$ = LOW) stops most of the internal logic (except the clocks MCO and SCO) to enable a power-down operation. After a reset, the internal sequencer starts and the conversions begin. To prevent the output of corrupted data, the outputs BUFO, SDO and PD0-13 are muted for 32 sample periods ($1/f_s$).

System Synchronization

(via CONVREADY pin)
To synchronize the connected system, the PCF5012 provides a CONVREADY output. Its transition indicates that a new sample can be taken from the data output and supplied to the data input. The PCF5012 is thus always the master for the sampling rate.

To allow internal data exchange, all I/O actions have to be completed three SCO cycles before the next transition of CONVREADY.

Package Selection (via SEL44 pin)

SEL44 has to be HIGH when the QFP44 package is used and LOW when the DIL28 package is used.

14-bit ADC/DAC converter

PCF5012

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	−0.5	+7.0	V
V_{DDA}	analog supply voltage	-0.5	+7.0	V
V_I	DC input voltage	-0.5	V_{DD} +0.5	V
V_I	DC input voltage	-	7	V
$I_{I(D)}$	DC input diode current	−10	+10	mA
V_O	DC output voltage	−0.5	V_{DD} +0.5	V
I_O	DC output current	−20	+20	mA
I_{DD}	DC supply current	-	60	mA
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C

14-bit ADC/DAC converter

PCF5012

DC CHARACTERISTICS

T_{amb} = −40 to +85 °C, f_s = 16 kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_D	supply voltage difference V_{DDA}/V_{DDD}, AGND/DGND		-	-	0.25	V
P_{DA}	supply dissipation (analog)		-	25	-	mW
P_{DD}	supply dissipation (digital)		-	100	-	mW
P_{DD}	supply dissipation (V_{DDD})	in reset	-	25	-	mW
I_{IL}	supply leakage current		-	*	-	
Reference generation						
V_{ref}	reference voltage (% of V_{DD})	note 1	48	50	52	
Z_{ref}	reference impedance		-	7.5	-	kΩ
Crystal oscillator						
gm	mutual conductance		-	*	-	mA/V
G_v	small signal voltage gain		-	*	-	
C_I	input capacitance		-	10	-	pF
C_O	output capacitance		-	10	-	pF
C_{FB}	feedback capacitance		-	5	-	pF
Logic inputs						
V_{IL}	input voltage LOW		-	-	+0.8	V
V_{IH}	input voltage HIGH		2.0	-	-	V
I_{IL}	input leakage current		−1.0	-	+1.0	μA
C_I	input capacitance		-	10	-	pF
Logic outputs						
V_{OL}	output voltage LOW	I_{OL} = 1 mA	-	-	+0.4	V
V_{OH}	output voltage HIGH	I_{OH} = 50 μA	+2.4	-	-	V
Master clock output (MCO)						
I_O	output current	V_O = 0.4 V	-	-	4	mA
Output $\overline{IOE}$ and SCO (with 50 pF load)						
I_O	output current	V_O = 0.4 V	-	-	2	mA
All other outputs (with 35 pF load)						
I_O	output current	V_O = 0.4 V	-	-	1	mA

Note to the DC characteristics

1. Any noise on V_{ref} directly modulates the analog signals.

* Value to be fixed.

14-bit ADC/DAC converter

PCF5012

AC CHARACTERISTICS

T_{amb} = -40 to +85 °C, f_s = 16 kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_{XTAL}	crystal frequency		3.6	8.0	8.4	MHz
External clock input (MCI) (note 1)						
f_{XTAL}	crystal frequency		3.6	8.0	8.4	MHz
t_{IH}	input time HIGH (% $1/f_{XTAL}$)		40	50	60	
t_r	rise time	0.8 to 2.0 V	-	-	15	ns
t_f	fall time	2.0 to 0.8 V	-	-	15	ns
Master clock output (MCO) (with 50 pF load)						
t_r	rise time	0.8 to 2.0 V	-	-	15	ns
t_f	fall time	2.0 to 0.8 V	-	-	15	ns
Output $\overline{IOE}$ and SCO (with 50 pF load)						
t_r	rise time	0.8 to 2.0 V	-	-	30	ns
t_f	fall time	2.0 to 0.8 V	-	-	30	ns
All other outputs (with 35 pF load)						
t_r	rise time	0.8 to 2.0 V	-	-	30	ns
t_f	fall time	2.0 to 0.8 V	-	-	30	ns
Delays referred to the appropriate clocks						
t_p	output propagation delay		5	-	-	ns
$t_{OHD;DAT}$	output hold time		5	-	-	ns
$t_{SU;DAT}$	input set-up time		5	-	-	ns
$t_{IHD;DAT}$	input hold time		0	-	-	ns
Clock inputs						
f_{SCI}	serial clock input (SCI) frequency		-	2	4	MHz
t_{DS}	data strobe ($\overline{DS}$) LOW		50	-	-	ns

Note to the AC characteristics

1. Any clock jitter directly modulates
   the analog signals.

14-bit ADC/DAC converter   **PCF5012**

DYNAMIC PERFORMANCE OF THE ADC

V_{DD} = 5 V; T_{amb} = 25 °C; f_s = 16 kHz; CLF1 = 220 pF ± 10%; CLF2 = 330 pF ± 10%; CLF3 = 30 pF;
unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{lref} (rms)	analog input reference level to achieve −1 dBFS (RMS value)	V_{DD} = 5 V; input = 1 kHz	1.09	1.1	1.3	V
Z_I	input impedance		33	45	67	kΩ
P_{SRR}	power supply rejection ratio	1 kHz	50	-	-	dB
f_{ch}	frequency characteristic 0 to 6.8 kHz 7 kHz	−1 dBFS input	 −1.2 −2.5	 - -	 +0.8 -	 dBFS dBFS
att	anti-aliasing attenuation 8 to 9 kHz 9 to 100 kHz > 100 kHz		 25 70 85	 - - -	 - - -	 dB dB dB
THD + N	total harmonic distortion and noise	−1 dBFS at 1 kHz	-	−70	−65	dB
THD + N	total harmonic distortion and noise	−20 dBFS at 1 kHz	-	−62	−60	dB
α	crosstalk from DAC		-	-	−60	dB
f_s	sampling rate	coupled to DAC	7.2	-	16.4	kHz
t_d	constant group delay		-	-	18	$1/f_s$
Δt	group delay deviation	f_s = 16 kHz	−15	-	+15	μs
MUTE	muting after reset to suppress random data		-	-	32	$1/f_s$

Note to the ADC characteristics

1. All specifications are given relative to digital Full Scale (0 dBFS). Digital full scale is defined as an input sinewave whose peak value reaches the positive full scale.

DYNAMIC PERFORMANCE OF THE DAC

V_{DD} = 5 V; T_{amb} = 25 °C; f_s = 16 kHz
CBUF = 220 pF ± 10%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{Oref} (rms)	analog output reference level (RMS value)	V_{DD} = 5 V; f = 1 kHz at −1 dBFS	0.97	1.0	1.03	V
	overload level	digital; full scale	-	-	0	dBFS
Z_{BUF}	load impedance at output		1.2	-	-	kΩ
C_L	direct capacitive load to AGND on buffer		-	-	50	pF
R_{fb}	internal buffer feedback resistor	note 1	19	21	23	kΩ
P_{SRR}	power supply rejection ratio	at 1 kHz	50	-	-	dB
f_{ch}	frequency characteristic	1 dBFS input				
	0 to 6.8 kHz		−1.2	-	−0.8	dBFS
	7 kHz		−2.5	-	-	dBFS
att	anti-imaging attenuation					
	8 to 9 kHz		25	-	-	dB
	9 to 119 kHz		70	-	-	dB
	> 119 kHz		30	-	-	dB
THD + N	total harmonic distortion and noise in 0 to 7 kHz band	−1 dBFS input	-	−82	−70	dB
THD + N	total harmonic distortion and noise in 0 to 7 kHz band	−20 dBFS input	-	−62	−60	dB
N_{idle}	idle noise up to 7 kHz	unweighted	-	-	−84	dBFS
α	crosstalk from the ADC		-	-	−60	dB
f_s	sampling rate	coupled to ADC	7.2	-	16.4	kHz
t_d	constant group delay		-	-	18	$1/f_s$
Δt	group delay deviation	f_s = 16 kHz	−15	-	+15	μs
MUTE	muting after RESET		-	-	32	$1/f_s$

Note to the DAC characteristics

1. This tolerance influences only the filter corner frequency, and not the output level.

14-bit ADC/DAC converter

PCF5012

DYNAMIC PERFORMANCE OF THE ADC/DAC IN CASCADE (ON THE SAME CHIP)

V_{DD} = 5 V; T_{amb} = 25 °C; f_s = 16 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD + N	overload point	digital full scale	-	0	-	dBFS
	total harmonic distortion and noise	0 to 7 kHz				
	−1 dBFS		-	−70	−65	dB
	−20 dBFS		-	-	−60	dB
f_N	single frequency noise	idle mode	-	-	−79	dBFS
N_{idle}	idle noise (RMS value)	unweighted				
	0 to 7 kHz		-	−75	-	dBFS
	0 to 20 kHz		-	−69	-	dBFS
t_d	absolute group delay		-	-	36	$1/f_s$
Δt	group delay deviation	f_s = 16 kHz	−0.3	-	+0.3	μs
ΔG	gain deviation from 0 dBFS to −65 dBFS	relative to −19 dBFS at 1 kHz	−0.3	-	+0.3	dB

14-bit ADC/DAC converter

PCF5012

TYPICAL SYSTEM CONFIGURATIONS

Serial Data Transfer

Figure 5 shows a possible configuration of the PCF5012 with a PCB5010/11 using the serial interface. The data transfer is a single channel transfer.

In this configuration, the PCF5012 provides the PCB5010/11 with the system clock (MCO) and also with the serial clock SCO = 128 x f_s for the serial data transmission. The system requires therefore only one crystal for the clock supply.

For systems, where more than one channel can be multiplexed onto the same serial I/O of a processor, the allocation of transfer time slots has to be defined. Figure 6 shows a possible configuration for a two-channel cascaded system. In this configuration PCF5012-1 starts the transfer of PCF5012-2 and also provides the supply of clock signals to the other units.

Such a cascaded system operates as follows:

PCF5012-1 is configured as a master (IOSTART = CONVREADY) and starts

the transfer of a data byte after the availability of a new set of data. During the serial transfer, the signal $\overline{\text{IOE}}$ of the PCF5012-1 is in the LOW condition. After the end of the serial transfer, to and from PCF5012 1, the signal $\overline{\text{IOE}}$ of PCF5012-1 changes to the HIGH condition.

PCF5012-2 (slave PCF5012) is triggered at the IOSTART input by the rising edge of $\overline{\text{IOE}}$ from PCF5012-1. After PCF5012-1 has finished its transfer PCF5012-2 starts its own serial data transfer using the common serial data lines SDI and
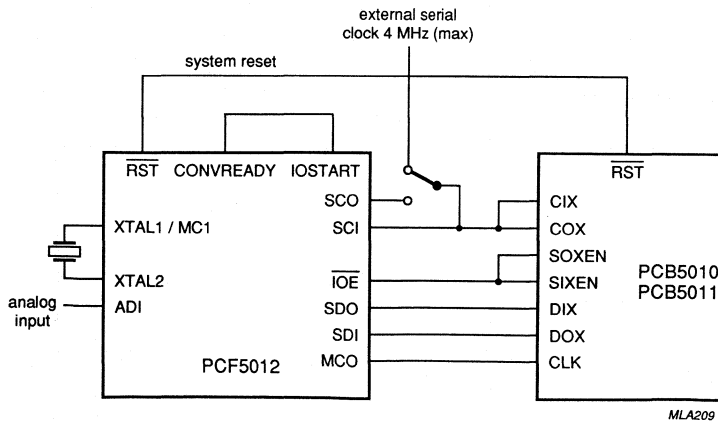
Fig.5 Single channel configuration PCF5012 and PCB5010/11.

14-bit ADC/DAC converter

PCF5012'

SDO. The transfer from PCF5012-2 to PCF5012-1 is therefore delayed by the transfer time of one data byte (15 SCI clock cycles). The signal processor detects, from the input flag IFA, which PCF5012 has transferred the data. Since the digital interfaces are asynchronous, in relation to the PCF5012 internal sequencing, only the transfer of the data blocks is delayed and not the actual conversion. To insure that all cascaded PCF5012's operate on the same sample, the first PCF5012's transfer starts directly after its internal data exchange.

Figure 7 shows a functional timing diagram of the described relationships. Such a cascaded system could be extended to more than two channels. It is a necessary condition, however, that the transfer of the data of all channels is completed within one sampling period. The serial clock frequency has to be chosen sufficiently high.

MLA210
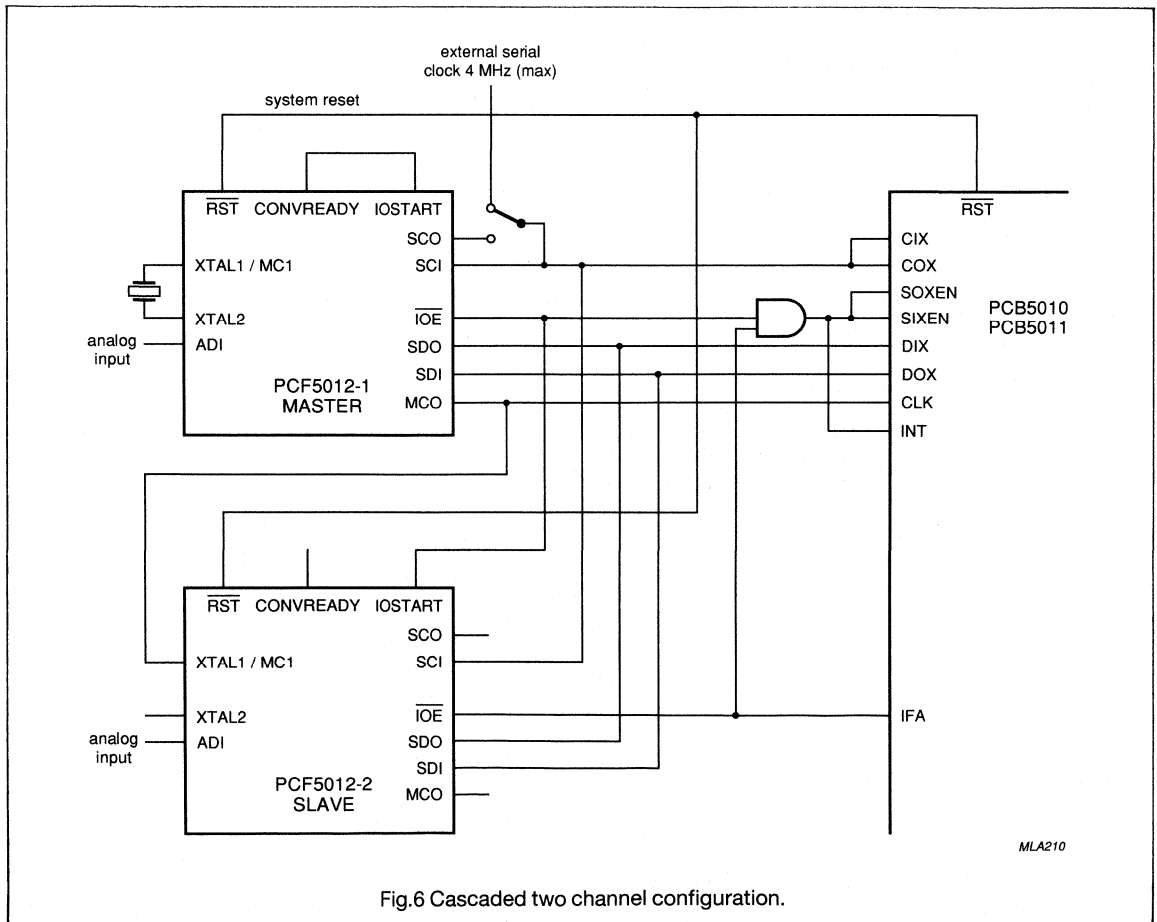
Fig.6 Cascaded two channel configuration.

14-bit ADC/DAC converter
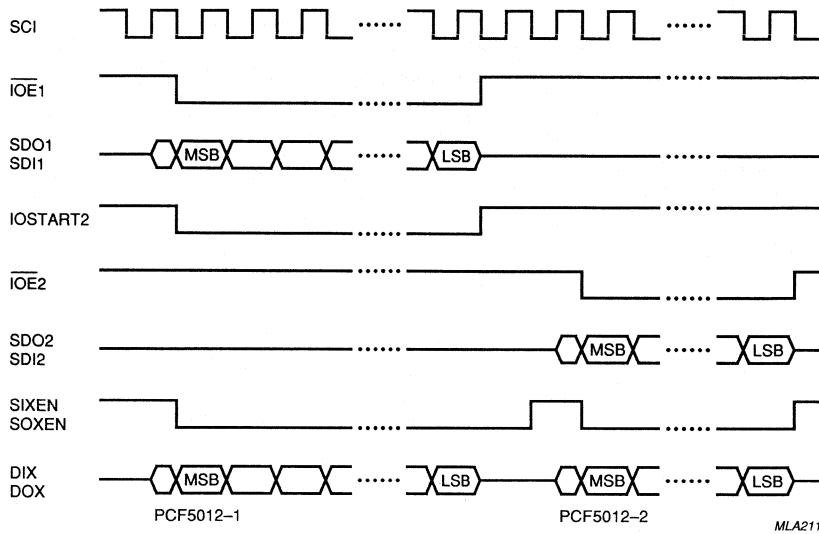
PCF5012

Fig.7 Timing of cascaded two channel configuration.

14-bit ADC/DAC converter

PCF5012

Parallel data transfer

Figure 8 shows a typical configuration for parallel data transfer.

In this configuration the signal processor PCB5010/11 communicates with a PCF5012 and, also, with an external data-RAM via the parallel interface.

In this configuration the signal $\overline{DS}$ is gated with an address line (A15) from the signal processor (memory mapped). As can be seen from the signal processor, a choice is thus made between the PCF5012 and the RAM. The PCF5012 requests data transfer via the interrupt-input (INT) of the signal processor. The processor then controls the parallel data exchange via R/$\overline{W}$ and $\overline{DS}$.
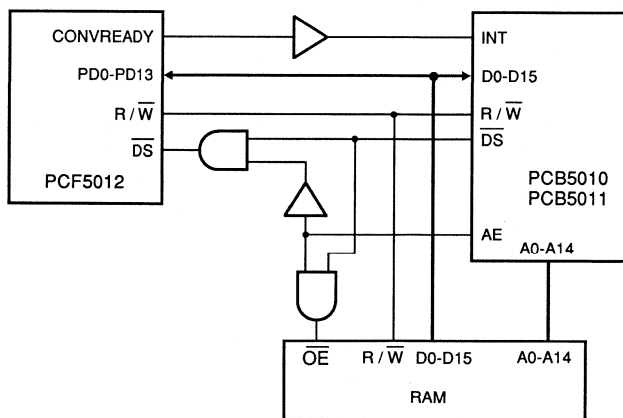
Fig.8 Possible configuration for parallel data transfer.

Data sheet	
status	Product specification
date of issue	November 1990

SCC68070
16/32-bit microprocessor

FEATURES

- CMOS technology
- 32-bit internal structure
- Enhanced bus error handling
- 4 decoded interrupt inputs
- 2 programmable interrupt inputs
- Decoded interrupt acknowledge
- Built-in clock generator - maximum 35 MHz crystal
- On-chip MMU; supporting virtual memory
- 2-channel DMA controller
- I^{2}C serial bus interface
- UART serial bus interface
- 16-bit timer/counter
- Two 16-bit match/count/capture registers
- Fully 68000 object code compatible
- Bus interface similar to 68000
- 56 powerful instruction types
- 5 basic data types
- 16 Mbyte addressing range
- 14 addressing modes
- Memory mapped I/O
- Vectored and auto-vectored interrupts
- 7 interrupt levels
- Maximum internal clock frequency: 17.5 MHz
- 84-pin PLCC or a 120-pin QFP package

GENERAL DESCRIPTION

The SCC68070 is a 16/32-bit central processing unit suitable for use in a large variety of applications. It is fully object code compatible with the 68000. By integrating standard and advanced peripheral functions on the SCC68070, system costs are drastically reduced.
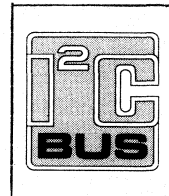
The internal architecture is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The SCC68070 includes powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a half crystal frequency clock signal for CPU and peripheral interfaces.

The on-chip MMU, if selected takes care of address translation and memory protection. Two DMA channels increase data throughput and the I^{2}C-bus interface allows easy and low-cost addition of peripherals. The SCC68070 also includes a UART interface. A built-in timer/counter with two independently programmable match/count/ capture registers, means that the SCC68070 can be programmed with two of the following options simultaneously:

- pulse generator
- external event counter
- reference timer

This document gives an overview of the basic functions, internal structure and electrical characteristics. For further details on the features and operation of the SCC68070 refer to "User Manual, Part 1 - Hardware".

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ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				CLOCK FREQUENCY (MHz)	TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE		
SCC68070CBA84	84	PLCC	plastic	SOT189CG, AGA	12.5	0 to 70
SCC68070CCA84	84	PLCC	plastic	SOT189CG, AGA	15.0	0 to 70
SCC68070CDA84	84	PLCC	plastic	SOT189CG, AGA	17.5	0 to 70
SCC68070ABA84	84	PLCC	plastic	SOT189CG, AGA	12.5	−40 to 85
SCC68070ACA84	84	PLCC	plastic	SOT189CG, AGA	15.0	−40 to 85
SCC68070ADA84	84	PLCC	plastic	SOT189CG, AGA	17.5	−40 to 85
SCC68070CBB	120	QFP	plastic	SOT220	12.5	0 to 70
SCC68070CCB	120	QFP	plastic	SOT220	15.0	0 to 70
SCC68070CDB	120	QFP	plastic	SOT220	17.5	0 to 70
SCC68070ABB	120	QFP	plastic	SOT220	12.5	−40 to 85
SCC68070ACB	120	QFP	plastic	SOT220	15.0	−40 to 85
SCC68070ADB	120	QFP	plastic	SOT220	17.5	−40 to 85

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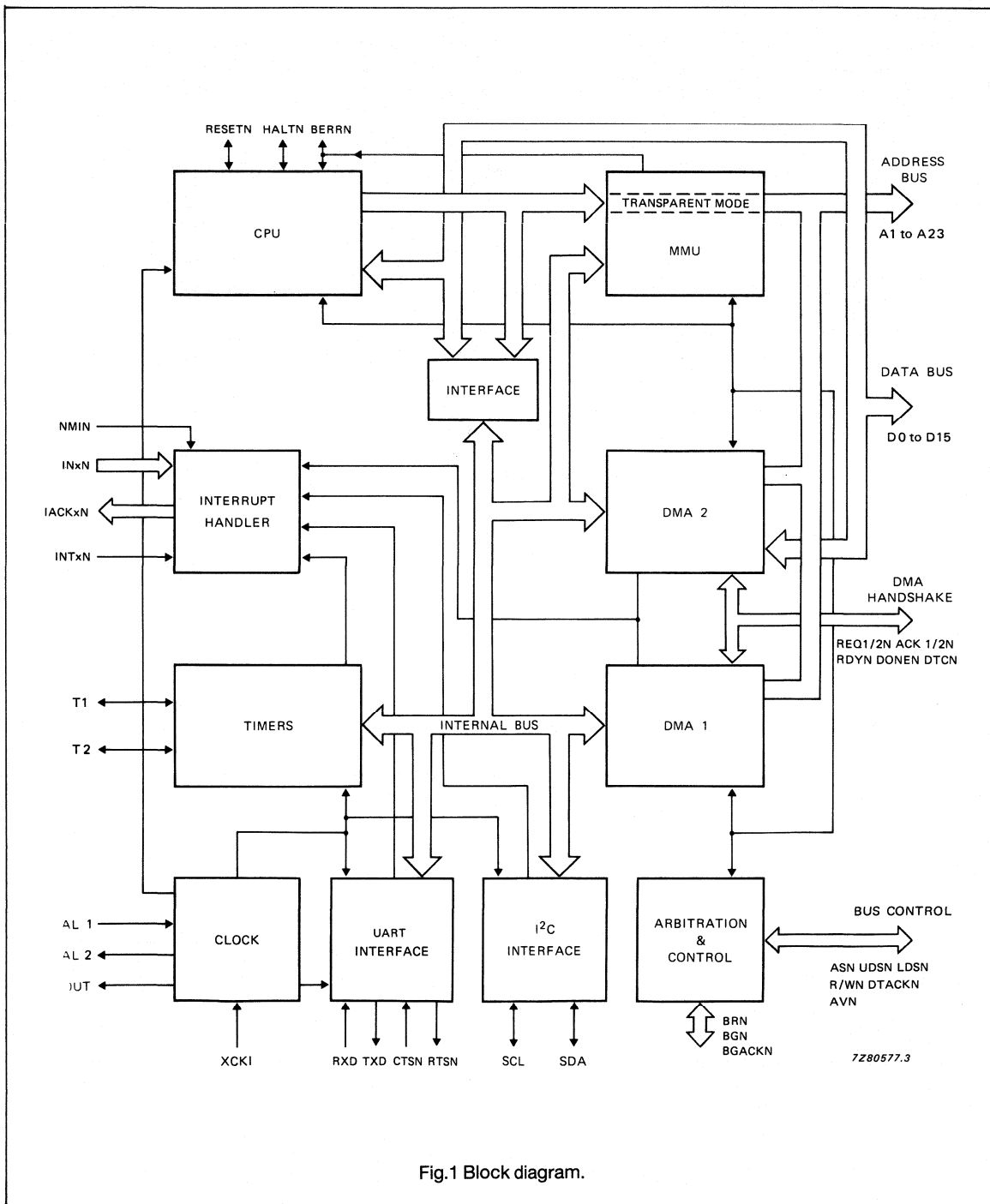
Fig.1 Block diagram.

16/32-bit microprocessor
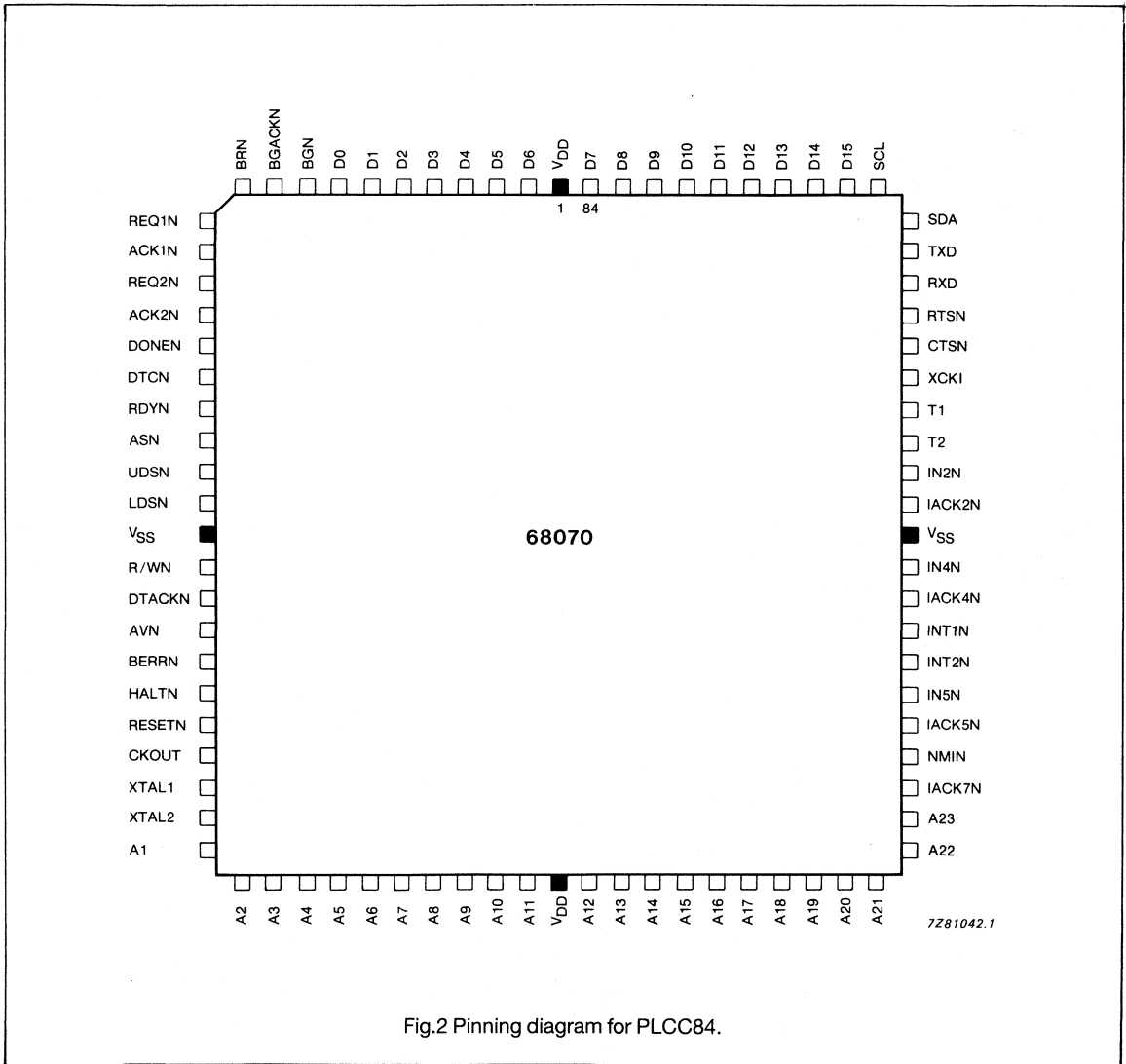
SCC68070

Fig.2 Pinning diagram for PLCC84.

16/32-bit microprocessor
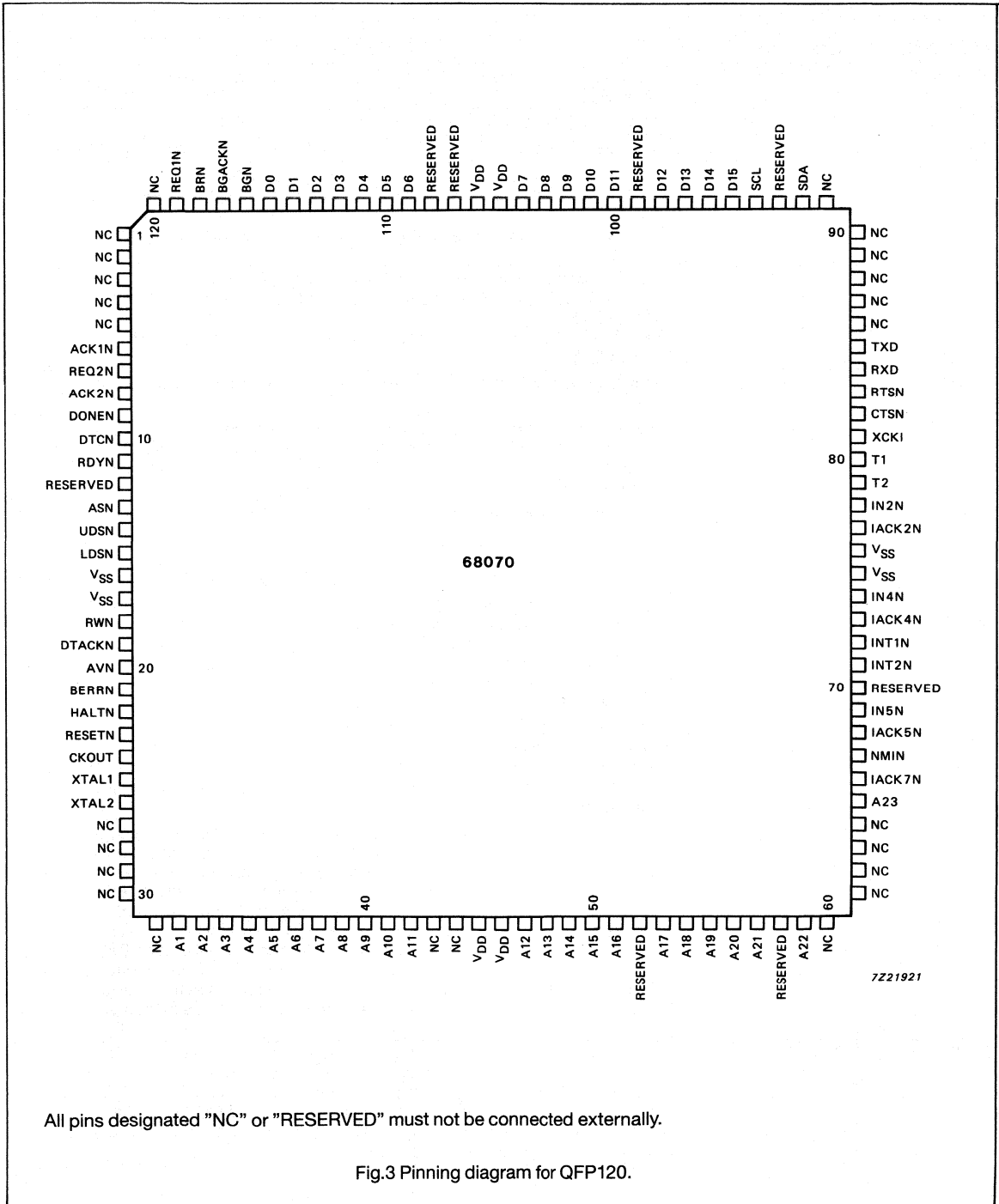
SCC68070

All pins designated "NC" or "RESERVED" must not be connected externally.

Fig.3 Pinning diagram for QFP120.

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Signal description (PLCC84)

MNEMONIC	TYPE	PIN NO.	FUNCTION
A1 to A23	O	32-42, 44-55	**Address bus** (active HIGH, 3-state). For direct addressing of 16 Mbytes of memory.
D0 to D15	I/O	8-2, 84-76	**Data bus** (active HIGH, 3-state, bidirectional). 16-bit wide.
ASN	O	19	**Address Strobe** (active LOW, 3-state). Indicates a valid address on the bus.
LDSN	O	21	**Lower Data Strobe** (active LOW, 3-state). Indicates that: - For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). - For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O	20	**Upper Data Strobe** (active Low, 3-state). Indicates that: - For a WRITE cycle, the data is valid on the lower half of the data bus (D8 to D15). -For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O	23	**Read** (active HIGH)/**Write** (active LOW). This controls the direction of data flow.
DTACKN	I	24	**Data Transfer Acknowledge** (active LOW). Asserted by the peripheral during CPU or DMA bus cycles when data is either received from or placed on the bus. If not asserted punctually, it causes the CPU or DMA controller to insert wait states.
BRN	I	11	**Bus Request** (active LOW). Asserted by wired-ORed external DMA devices that request bus ownership.
BGN	O	9	**Bus Grant** (active LOW). A daisy chain output that is asserted by the SCC68070 when the bus is granted by the CPU and the DMA does not have a bus request pending.
BGACKN	I/O	10	**Bus Grant Acknowledge** (active LOW, open drain). Asserted by any DMA device (internal or external) that has control of the bus. As long as this line is held LOW externally, the SCC68070 will hold the bus signals in the high impedance state. When BGACKN is released, the SCC68070 will have access to the bus. Interrupts cannot be serviced while BGACKN is held LOW.
RESETN	I/O	28	**Reset** (active LOW, open drain, bidirectional). If asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the Reset instruction resets external hardware.
HALTN	I/O	27	**Halt** (active LOW, open drain, bidirectional). If asserted externally together with RESETN, it causes the SCC68070 to enter the Reset state. If asserted alone, it will cause the CPU or DMA controller to stop after completion of the current bus cycle. If HALTN and BERRN are asserted together, the CPU will complete the current bus cycle, stop operation, and place all 3-state lines in their high impedance state until HALTN and BERRN have been released, and then it will re-run the same bus cycle. BERRN should be released before HALTN. As long as HALTN is held LOW all control signals are inactive and all 3-state lines are placed in their high impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault) the processor drives this line LOW.
BERRN	I/O	26	**Bus Error** (active LOW, open drain). If this line is asserted during a bus cycle, it indicates that there was a fault in the bus cycle access. If asserted together with HALTN, the same bus cycle will re-run after both HALTN and BERRN have been released. If BERRN is asserted alone, the SCC68070 will start bus-error exception processing. BERRN is driven LOW by the SCC68070 when the MMU indicates a bus error.

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MNEMONIC	TYPE	PIN NO.	FUNCTION
INT1N, INT2N	I	61, 60	**Latched Interrupt inputs** (active LOW). A LOW level of ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable.
IN2N, IN4N, IN5N	I	66, 63, 59	**Decoded Interrupt priority inputs** (active LOW). IN2N has the lower and IN5N has the higher priority.
NMIN	I	57	**Non-maskable interrupt (level 7)** (active LOW). While the other interrupts may be masked (disabled), this interrupt is always enabled.
IACK2N, IACK4N, IACK5N, IACK7N	0	65, 62, 58, 56	**Decoded Interrupt acknowledge** (active Low). Asserted during an interrupt acknowledge sequence to indicate to a peripheral that its interrupt request is being serviced.
AVN	I	25	**Autovectored interrupts** (active LOW). If held LOW during the interrupt acknowledge sequence, the processor calculates the appropriate vector from a fixed vector table. If kept HIGH, the peripheral must provide an 8-bit vector number.
V_{DD}	-	1, 43	Supply voltage + 5.0 V nominal.
V_{SS}	-	22, 64	Ground.
XTAL1, XTAL2	I	30, 31	**External crystal inputs**. XTAL1 can be used as a clock input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O	29	**Clock out**. This is the reference from the internal system clock.
REQ1N, REQ2N	I	12, 14	**DMA Request** (active LOW). These are inputs from I/O devices requesting service from the DMA controller and causes it to request control of the bus. In burst mode, the inputs are level sensitive and the DMA controller releases the bus after REQ1N (or REQ2N) becomes active and the current DMA cycle is completed. In cycle-stealing mode, REQ1N or REQ2N inputs are triggered by a negative pulse. This pulse must occur at least one clock cycle before DTCN is asserted to ensure continuous transfer.
ACK1N, ACK2N	O	13, 15	**DMA Request Acknowledge** (active LOW). ACK1N (or ACK2N) is asserted by the DMA controller to indicate that it has acquired the bus and the requested device bus cycle is now beginning. It is active at the beginning of every device cycle together with ASN, and is deactivated at the end of every device bus cycle.
RDYN	I	18	**Device Ready** (active LOW). The requesting device asserts RDYN to indicate to the DMA controller that valid data has either been stored or put on the bus. If RDYN remains inactive, it indicates that the data has neither been stored nor put on the bus, causing the DMA controller to insert wait states. RDYN can be held LOW permanently if the device is fast enough, indicating that the device is always ready and so no wait states are required. RDYN is not monitored by Channel 2 in the dual address mode.
DTCN	O	17	**Device Transfer Complete** (active LOW, open drain). In DMA mode DTCN is asserted by the DMA controller to indicate to the device that the requested data transfer is complete. On a write-to-memory operation, it indicates that the data provided by the device has been stored successfully. On a read-from-memory operation, it indicates that the data from memory is present on the data bus and should be latched.
DONEN	I/O	16	**Done** (active LOW, open drain). With DONEN as an output, the DMA controller asserts it simultaneously with the ACK1N (or ACK2N) output to indicate to the device that the transfer count is zero and therefore, the DMA controller's operation is complete. If, as an input, DONEN is asserted by the device before the transfer count reaches zero, it causes the DMA controller to abort the operation and generate an interrupt request (if the interrupts are enabled).

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MNEMONIC	TYPE	PIN NO.	FUNCTION
SCL	I/O	75	**Serial Clock** (open drain). SCL is the clock signal for the I²C-bus operation. It is either driven by the SCC68070 when the I²C interface is in the master mode, or is the clock input if the I²C interface is in the slave mode.
SDA	I/O	74	**Serial Data** (open drain). SDA is the data signal for the I²C-bus.
T1, T2	I/O	68, 67	**Timers 1 and 2** (3-state). These are the I/O signals for the capture timers of channels 1 and 2 respectively. They can be programmed as either outputs for pulses or inputs for count cycles and events.
RXD	I	72	**Receive Data**. RXD is the data input for the UART serial interface.
TXD	O	73	**Transmit Data**. TXD is data output for the UART serial interface.
RTSN	O	71	**Request To Send** (active LOW). This output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN	I	70	**Clear To Send** (active LOW). This input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected together if no control lines are needed.
XCKI	I	69	**External clock**. When selected, XCKI is the clock input for the UART serial interface. This signal can be used either: - to generate special baud rates or, - when a crystal frequency other than 19.6608 MHz is used by the SCC68070, an external clock of 4.9152 MHz (or 9.8304 for 38200 bauds) can be connected to this input to generate the standard baud rates.

Note

The signal descriptions given for the PLCC84 package also apply to the QFP120 package. However, the pinning arrangement for the QFP120 is different, as can be seen in Fig.3.

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_I	Input voltage on any pin with respect to ground (V_{SS})		−0.3	
I_I, I_0	Input, output current	-	±10	mA
P_{tot}	Total power dissipation	-	2	W
T_{stg}	Storage temperature range	−55	+ 150	°C
T_{amb}	Operating ambient temperature ranges*	0 −40	+ 70 + 85	°C °C

* Devices are availible in two temperature ranges; see
   Ordering information.

Notes to Limiting Values and Electrical characteristics

1. Stresses above those listed in the Absolute Maximum
   System may cause permanent damage to the device.
   These are stress ratings only and do not mean that
   the device will operate at these or other conditions
   above those given in the operation section.
2. For operating at elevated temperatures, the device
   must be derated based on a 150°C maximum
   junction temperature.
3. This product contains circuitry specifically designed
   to protect its internal devices from excessive static
   charge. Nevertheless it is recommended that
   conventional precautions be taken to avoid applying
   any voltage above the rated maxima.
4. Parameters are valid over specified temperature
   range.
5. All voltages are measured with ground as reference
   (GRD). For testing, all input signals swing between
   0.4 and 2.4 V with a transmission time of 5 ns
   maximum. All time measurements are made with
   input and output voltages of 0.8 and 2.0 V as
   appropriate.
6. On clock input XTAL1 when an external clock is used.

7. All timing measurements have CKOUT as a reference
   for both internal oscillator and external clock input
   modes. The device has been designed to be used
   with a 35 MHz crystal but the minimum crystal
   frequency specified is 8 MHz. All timing
   measurements except number 1 are specified at
   19.6608, 25, 30 and 35 MHz.
8. Actual value depends on clock period.
9. After V_{DD} has been applied for 100 ms.
10. If the asynchronous setup time (#41A) requirements
    are met, the DTACKN LOW-to-data setup time (#31)
    requirements can be ignored. The data must only
    satisfy the data-in to clock-LOW setup time (#27) for
    the following cycle.
11. If the asynchronous setup time (#41A) requirements
    are met, for both DTACKN and BERRN, then #42 may
    be 0 ns.
12. All timing diagrams should only be referred to in
    regard to edge-to-edge measurements of the timing
    specifications. They are not intended as a functional
    description of the input and output signals. Refer to
    the functional description and related diagrams for
    device operation.

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DC CHARACTERISTICS

V_{DD} = 5.0 V ±10%; V_{SS} = 0 V; T_{amb} = 0 to + 70 ºC or −40 to + 85 ºC, dependent on type number. (See Figs.44 to 47 and notes 4 and 5).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{IH}	Input voltage HIGH, all inputs except XTAL1, XTAL2, SDA, SCL		2.0	V_{DD}	V
V_{IH1}	XTAL1	V_{DD} = 5.5 V	0.8V_{DD}	V_{DD}	V
V_{IH2}	SDA, SCL	-	3.0*	V_{DD}	V
VI_L	Input voltage LOW, all inputs except SDA, SCL	-	V_{SS}-0.3	0.8	V
V_{IL2}	SDA, SCL	V_{DD} = 4.5 V	V_{SS}-0.3	1.5	V
I_{LI}	Input leakage current RXD, CTSN, XCKI, DTACKN, INT1N, INT2N, REQ1N, REQ2N, RDYN, IN2N, IN4N, IN5N, NMIN, AVN, XTAL1	V_{DD} = 5.25 V V_{IN} = 5.25 V **	-	20	μA
I_{TSI}	3-state (off-state) input current A1-A23, D0-D15, ASN, LDSN, R/WN, UDSN, T1, T2	V_{IN} = 2.4/0.4 V	-	20	μA
I_{ODI}	Open-drain (off-state) input current BGACKN, RESETN, HALTN, BERRN, DTCN, DONEN, SCL, SDA	V_{DD} = 5.25 V	-	20	μA
V_{OH}	Output voltage HIGH A1-A23, DO-D15, ASN, BGN, LDSN, R/WN, UDSN, T1, T2, TXD, RTSN, ACKN1N, ACKN2N, IACKN2,4,5,7N	I_{OH} = 400 μA	2.4	-	V
V_{OH}	CKOUT	I_{OH} = 400 μA	0.8V_{DD}	-	V
V_{OL}	Output voltage LOW HALTN, BERRN, IACKN2,4,5,7, A1-A23, BGN, BGACKN, ACKN1N, ACKN2N, RESETN, T1, T2, RTSN, ASN, D0-D15, LDSN, R/WN, UDSN, DTCN, DONEN	I_{OL} = 3.2 mA	-	0.5	V
V_{OL}	CKOUT	I_{OL} = 3.2 mA	-	0.45	V
V_{OL}	SDA, SCL	I_{OL} = 3.0 mA	-	0.45	V
I_{DD}	Current consumption	CKOUT = 10 MHz	-	75	mA
		CKOUT = 15 MHz	-	112	mA
		CKOUT = 17.5 MHz	-	130	mA
C_i	Input capacitance	V_{IN} = 0V, T_{amb} = 25 ºC frequency = 1 MHz		20	pF

* Not tested, applied by external pullups.

** V_{IN} = enforced voltage.
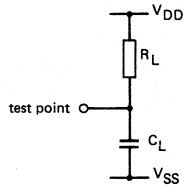
test point	R_L (kΩ)	C_L (pF)
RESETN	1.2	130
HALTN	1.2	130
SDA	1.4	400
SCL	1.4	400
BGACKN	1.2	130
DONEN	1.2	130
BERRN	1.2	130
DTCN	1.2	130

7Z81032.3

Fig.44 Open drain, bidirectional test loads.
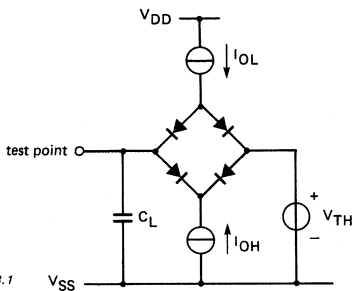
$C_L = 130$ pF (including all parasitics) exept CKOUT for which $C_L = 50$ pF

$V_{TH} = 1,6$ V   system load threshold voltage at which dynamic loads (I_{OL} and I_{OH}) switch; see d.c. characteristics

7Z81033.1

Fig.45 Remaining test loads.
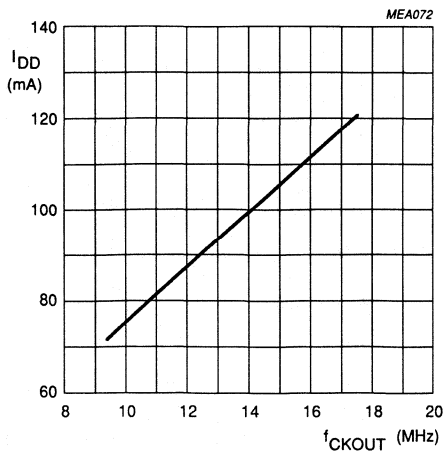
Fig.46 I_{DD} (max.) as a function of frequency.
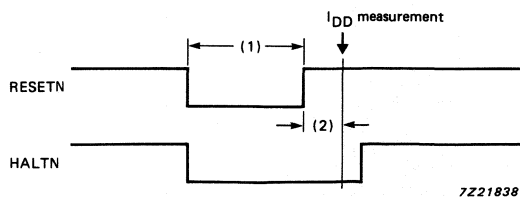
1. ≥ 400 t_{CYC}.
2. ≥ 10 ms.

Fig.47 I_{DD} measurement.

16/32-bit microprocessor

SCC68070

AC CHARACTERISTICS

$V_{DD} = 5$ V ±10%, $V_{SS} = 0$ V, $T_{amb} = 0$ to + 70 °C or –40 to + 85 °C (dependent on type number), C_{load} on
CKOUT = 50 pF (see Figures 48 to 51).

SYMBOL	PARAMETER	NO.	f_{XTAL1}=19.6 MHz		f_{XTAL1}=25 MHz		f_{XTAL1}=30 MHz		f_{XTAL}=35 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{CYC}	Crystal or input clock period	1	50	125	40	125	33	125	28.5	125	ns
t_{XHCV}	XTAL HIGH to CKOUT HIGH or LOW	1A	8	96	5	45	5	40	5	30	ns
t_{COL}2	CKOUT, LOW level	2	33	-	25	-	20	-	15	-	ns
t_{COH}	CKOUT, HIGH level	3	33	-	25	-	20	-	15	-	ns
t_{COf}	CKOUT fall-time	4	-	10	-	10	-	10	-	10	ns
t_{COr}	CKOUT rise-time	5	-	12	-	10	-	10	-	10	ns
t_{CLAV}	CKOUT LOW to address valid	6	-	55	-	50	-	50	-	45	ns
t_{CHAZx}	CKOUT HIGH to address/data, high-impedance (max.)	7	-	55	-	55	-	55	-	55	ns
t_{CHAZn}	CKOUT HIGH to address invalid (min.)	8	0	-	0	-	0	-	0	-	ns
t_{CHSL}	CKOUT HIGH to ASN, DSN LOW	9	0	45	0	45	0	45	0	30	ns
t_{AVSL}	Address to ASN/DSN (read), ASN (write) LOW	11[8]	20	-	10	-	10	-	10	-	ns
t_{SLSH}	CKOUT LOW to ASN, DSN HIGH	12	0	55	0	45	0	45	0	45	ns
t_{SHAZ}	ASN, DSN HIGH to address invalid	13[8]	20	-	10	-	10	-	10	-	ns
t_{SL}	ASN/DSN (read), ASN (write) LOW level	14[8]	200	-	160	-	130	-	105	-	ns
t_{DSL}	DSN LOW level (write)	14A[8]	100	-	80	-	65	-	50	-	ns
t_{SH}	ASN, DSN HIGH level	15	100	-	80	-	70	-	60	-	ns
t_{CHSZ}	CKOUT HIGH to ASN, DSN high impedance	16	-	55	-	55	-	50	-	50	ns
t_{SHRH}	ASN, DSN HIGH to R/WN HIGH (read)	17[8]	20	-	10	-	10	-	10	-	ns
t_{CHRH}	CKOUT HIGH to R/WN HIGH	18	0	55	0	45	0	45	0	45	ns
t_{CHRL}	CKOUT HIGH to R/WN LOW (write)	20	-	55	-	45	-	45	-	45	ns
t_{AVRL}	Address valid to R/WN LOW (write)	21[8]	0	-	0	-	0	-	0	-	ns
t_{CLSL}	R/WN LOW to DSN LOW (write)	22[8]	55	-	30	-	25	-	20	-	ns
t_{CLDO}	CKOUT LOW to data out valid (write)	23	-	50	-	45	-	45	-	45	ns

Note. 'cp' denotes clock pulses.

16/32-bit microprocessor

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SYMBOL	PARAMETER	NO.	f_{XTAL1}=19.6 MHz		f_{XTAL1}=25 MHz		f_{XTAL1}=30 MHz		f_{XTAL}=35 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SHDO}	ASN, DSN HIGH to data out invalid (write)	25[8]	20	-	15	-	15	-	15	-	ns
t_{DOSL}	Data out valid to DSN LOW (write)	26[8]	20	-	15	-	15	-	15	-	ns
t_{DICL}	Data in to clock LOW (set-up time, read)	27[10]	10	-	10	-	5	-	5	-	ns
t_{SHDAH}	ASN, DSN HIGH to DTACKN, RDYN, AVN HIGH	28[8]	0	190	0	150	0	120	0	90	ns
t_{SHDI}	ASN, DSN HIGH to data invalid (hold time, read)	29	0	-	0	-	0	-	0	-	ns
t_{SHBEH}	ASN, DSN HIGH to BERRN HIGH	30	0	-	0	-	0	-	0	-	ns
t_{DCLDI}	DTACKN LOW to data in (set-up time, read)	31[8/10]	-	65	-	50	-	45	-	40	ns
t_{RHrf}	HALTN and RESETN input transition time	32[9]	0	200	0	200	0	200	0	200	ns
t_{CHGL}	CKOUT HIGH to BGN LOW	33	-	55	-	50	-	50	-	50	ns
t_{CHGH}	CKOUT HIGH to BGN HIGH	34	-	55	-	50	-	50	-	50	ns
t_{BRLGL}	BRN LOW to BGN LOW	35	1.5	3.5 +80	1.5	3.5 +70	1.5	3.5 +70	1.5	3.5 +70	cp ns
t_{BRHGH}	BRN HIGH to BGN HIGH	36	1.5	2.5 +80	1.5	2.5 +70	1.5	2.5 +70	1.5	2.5 +70	cp ns
t_{GALGH}	BGACKN LOW to BGN HIGH	37	1.5	2.5 +80	1.5	2.5 +70	1.5	2.5 +70	1.5	2.5 +70	cp ns
t_{GLZ}	BGN LOW to bus high impedance (ASN HIGH)	38	-	55	-	50	-	50	-	50	ns
t_{GH}	BGN HIGH level	39	1.5	-	1.5	-	1.5	-	1.5	-	cp
t_{BGL}	BGACKN width	40	1.5	-	1.5	-	1.5	-	1.5	-	cp
t_{ASI}	Asynchronous set-up time	41	25	-	25	-	25	-	25	-	ns
t_{ASDT}	Asynchronous set-up time for DTACKN, AVN, BERRN, HALTN, RDYN	41A[10]	25	-	10	-	10	-	10	-	ns
t_{BELDAL}	BERRN (input) LOW to DTACKN LOW	42[11]	20	-	15	-	15	-	15	-	ns
t_{CHDO}	CKOUT HIGH to Data OUT invalid (write)	43	0	-	0	-	0	-	0	-	ns
t_{RLDL}	R/WN LOW to data bus driven	44	20	-	10	-	10	-	10	-	ns

16/32-bit microprocessor

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SYMBOL	PARAMETER	NO.	f_{XTAL1}=19.6 MHz		f_{XTAL1}=25 MHz		f_{XTAL1}=30 MHz		f_{XTAL}=35 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{HRPW}	HALTN/RESETN pulse width	45	10	-	10	-	10	-	10	-	cp
	REQx set-up before CKOUT LOW	46	25	-	10	-	10	-	10	-	ns
	ACKxN LOW from CKOUT HIGH	47	0	50	0	50	0	50	0	50	ns
	REQxN hold after CKOUT LOW	48	10	-	10	-	10	-	10	-	ns
	DTCN LOW from CKOUT HIGH	49	-	50	-	50	-	50	-	50	ns
	ASN, LDSN, UDSN HIGH from DTCN LOW	50	0	-	0	-	10	-	10	-	ns
	ACKxN HIGH from CKOUT HIGH	51	-	55	-	50	-	50	-	50	ns
	DTCN non-active to CKOUT HIGH	52	-	45	-	40	-	40	-	40	ns
	DONEN (output) LOW from CKOUT HIGH	53	-	45	-	40	-	40	-	40	ns
	DONEN (output) non-active from CKOUT HIGH	54	-	55	-	55	-	55	-	55	ns
	DONEN (input) set-up LOW before CKOUT LOW	56	25	-	10	-	10	-	10	-	ns
	DONEN (input) hold LOW after CKOUT HIGH	57	10	-	10	-	10	-	10	-	ns
	REQ LOW to BGACKN (output) LOW	58	3.5	-	3.5	-	3.5	-	3.5	-	cp
	CKOUT LOW to BERRN (output) LOW	59	-	50	-	40	-	40	-	40	ns
	CKOUT LOW to BERRN (output) non-active	60	-	45	-	45	-	45	-	45	ns
	CKOUT HIGH to BGACKN (output) LOW	61	-	60	-	60	-	60	-	60	ns
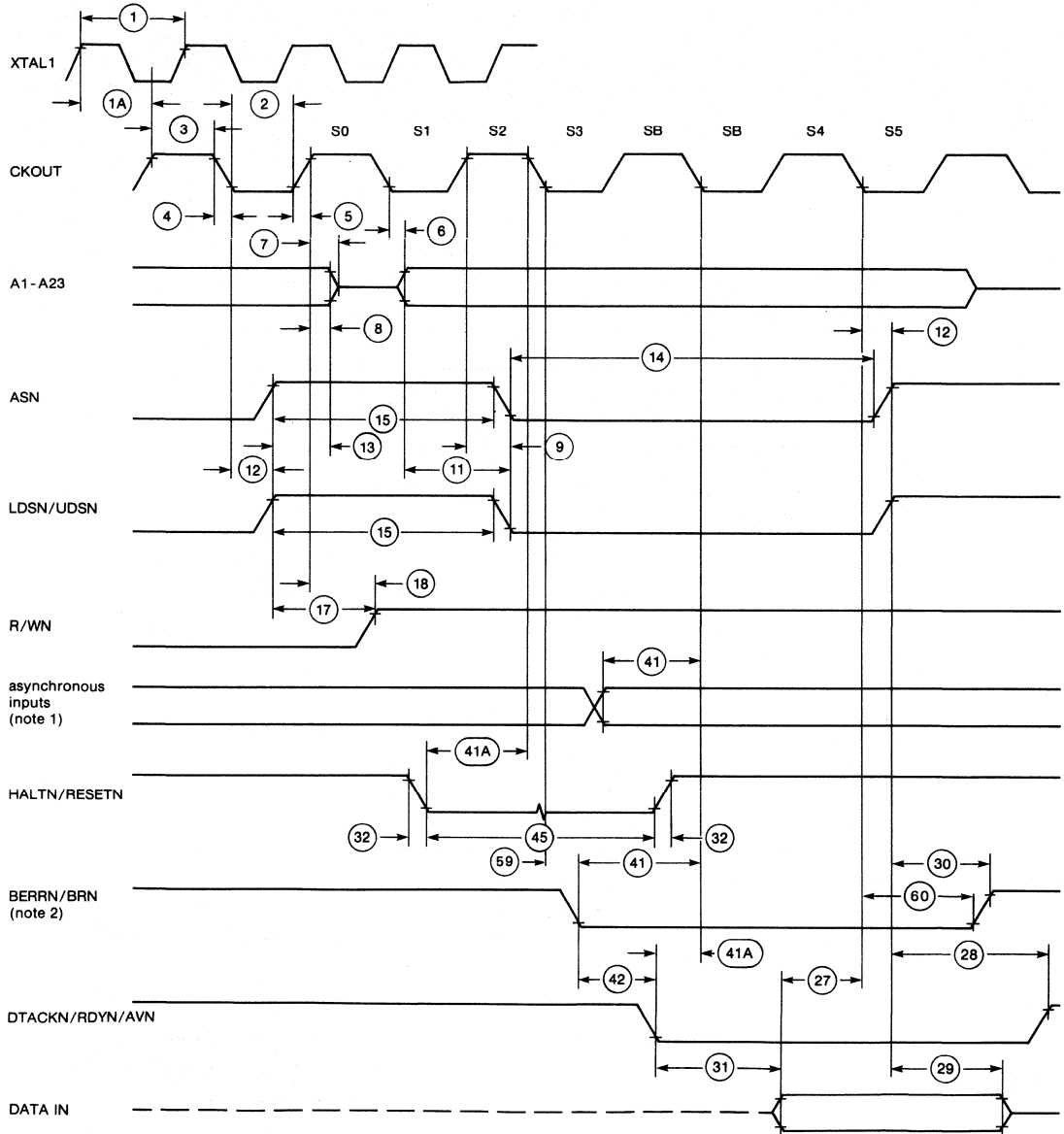
7Z81046.1

Notes to Fig.48

1. Setup time for the asynchronous inputs and AVN guarantees their recognition at the next falling edge of the clock.

2. BRN need fall at this time only to ensure being recognized at the end of this bus cycle. When BERRN is driven during a faulty MMU cycle, an additional error cycle (SE) is inserted in between SB and S4.

Fig.48 Read cycle timing.

16/32-bit microprocessor
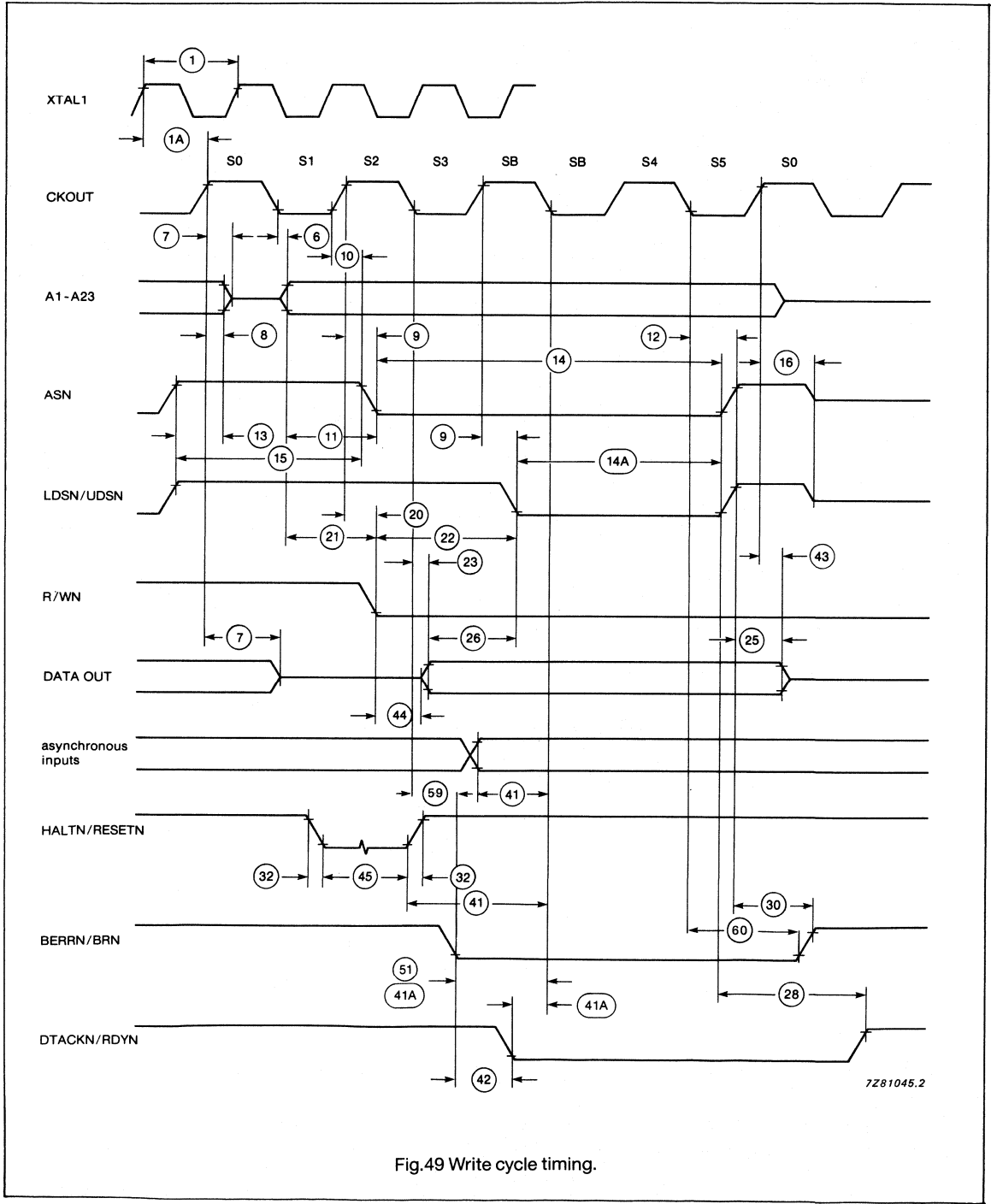
SCC68070

Fig.49 Write cycle timing.

7Z81045.2

16/32-bit microprocessor
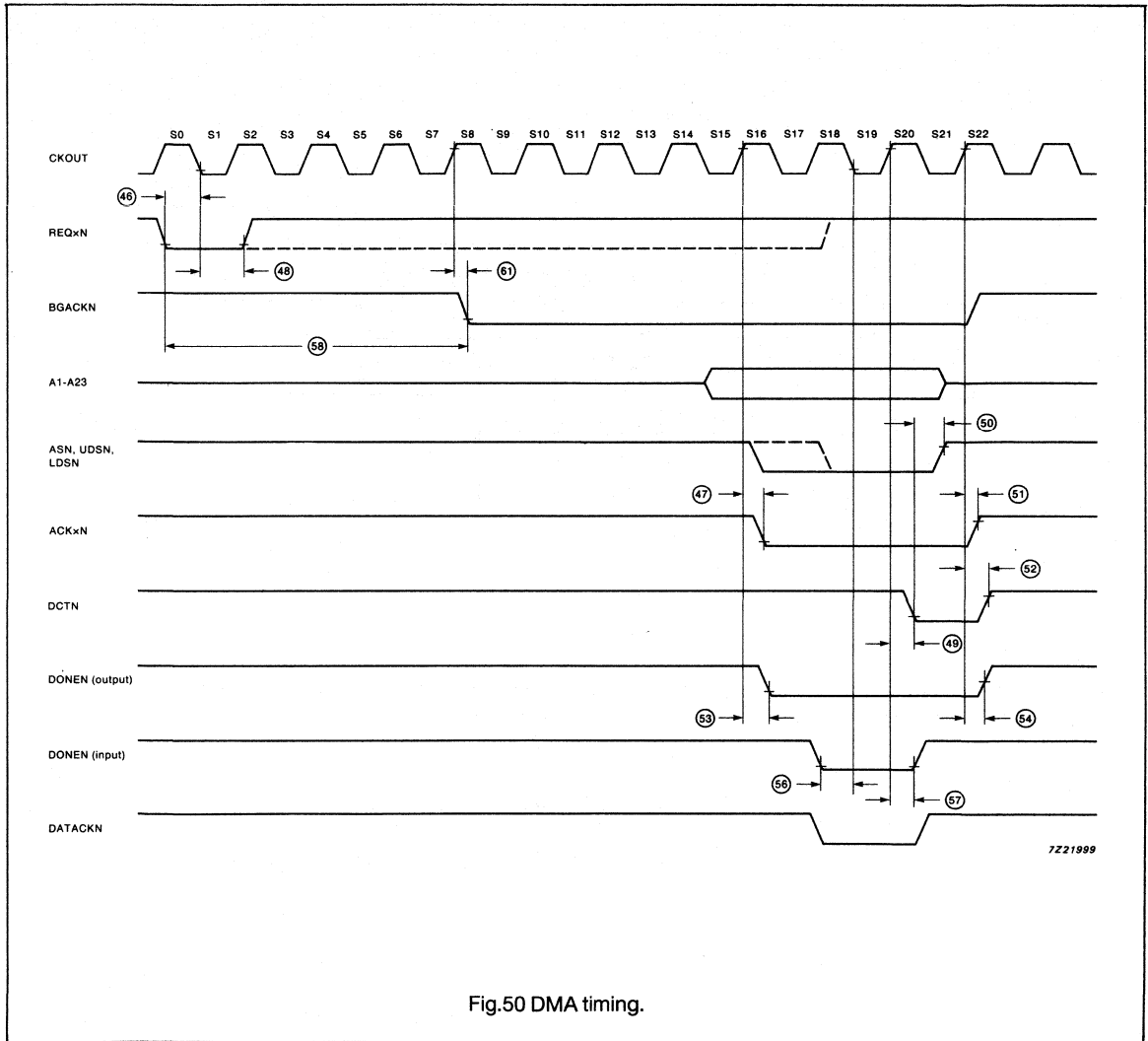
SCC68070

Fig.50 DMA timing.

16/32-bit microprocessor

SCC68070
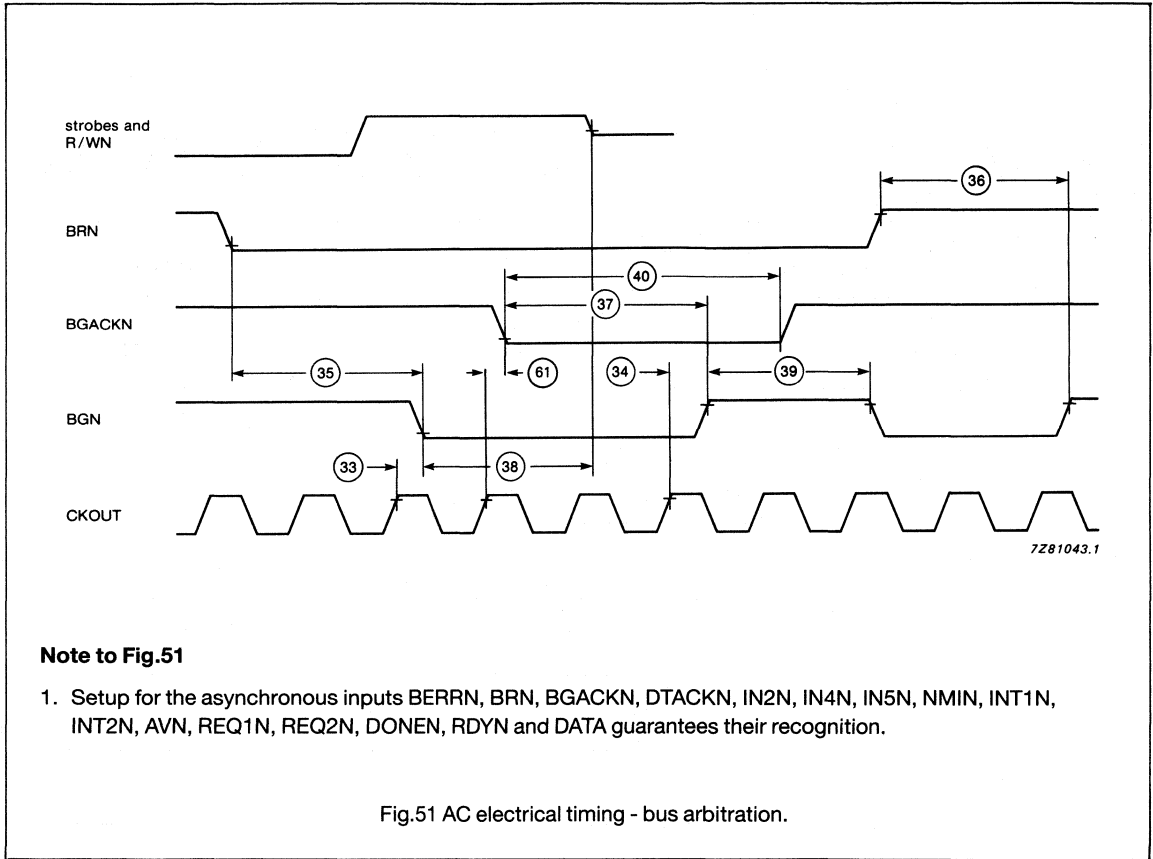
Note to Fig.51

1. Setup for the asynchronous inputs BERRN, BRN, BGACKN, DTACKN, IN2N, IN4N, IN5N, NMIN, INT1N, INT2N, AVN, REQ1N, REQ2N, DONEN, RDYN and DATA guarantees their recognition.

Fig.51 AC electrical timing - bus arbitration.
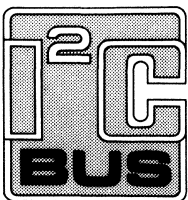
Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

PACKAGE INFORMATION

Package outlines
Soldering

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)
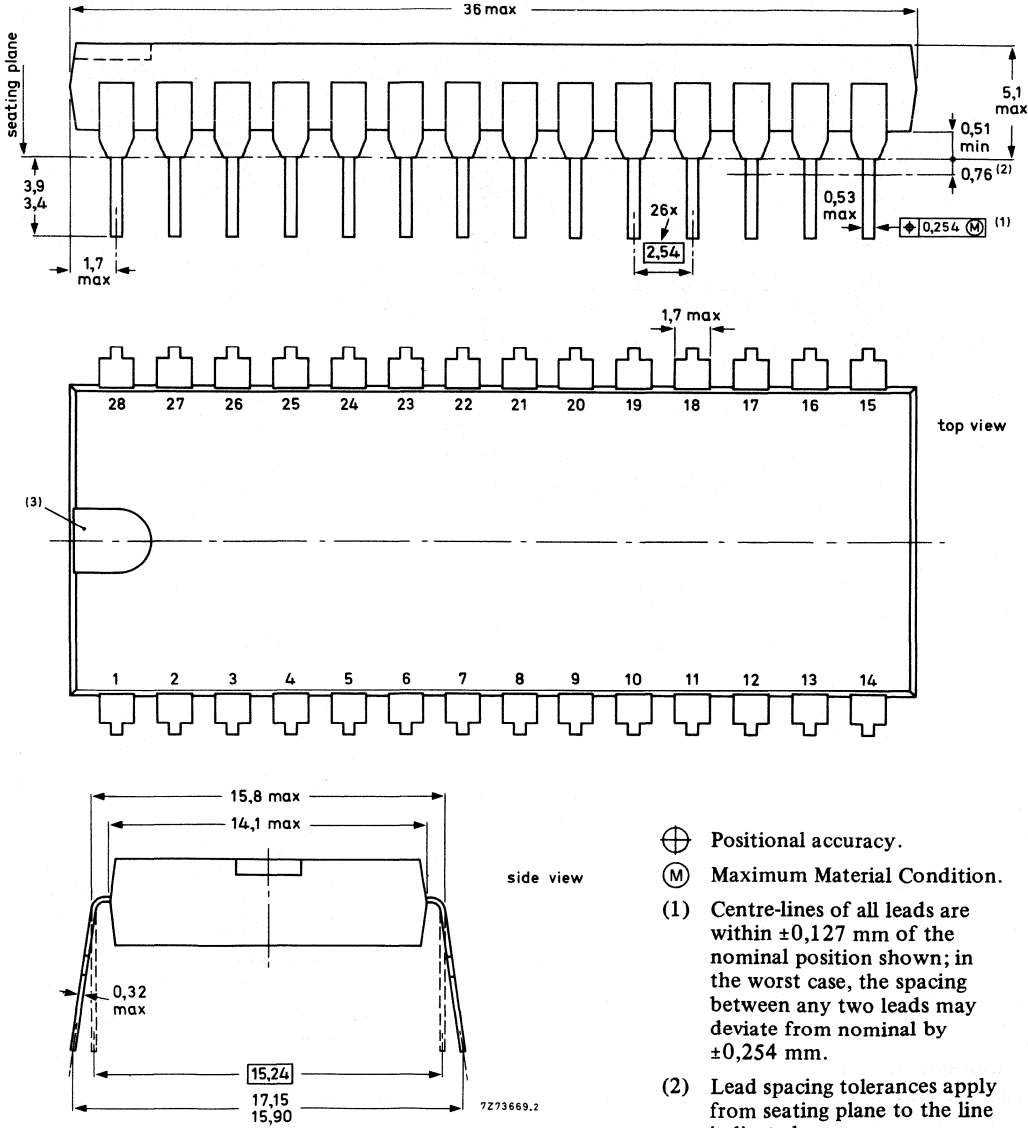
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); (SOT187AA, AGA)

45°

0.51 max
(3x)

A

6 1 44 40

1.07 min

7

pin 1 index

39

A

1.27

2.15 max

17

29

18 28

□ 16.66 max

□ 17.65 max

⊕ 0.18 Ⓜ

4.57 max

1.42
1.07

0.53
0.33

0.81 max

16.0
14.99

3.04 max

A–A

R 1.14
0.64

45°

⬦ 0.10

seating plane

0.51 min

7Z25134.1

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm
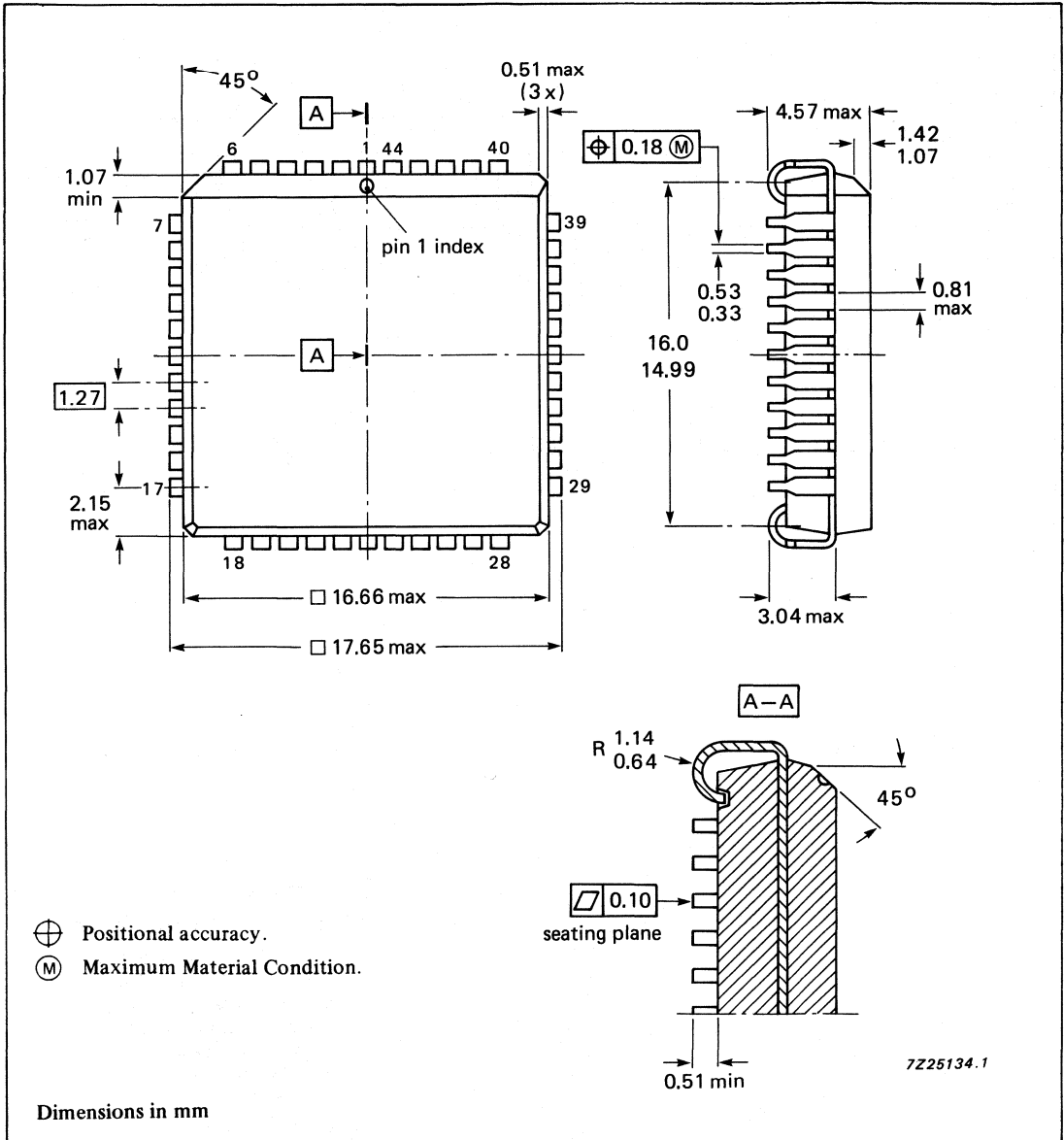
68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); (SOT188AA, AGA)

Positional accuracy.

Maximum Material Condition.

Dimensions in mm

7Z25139.1
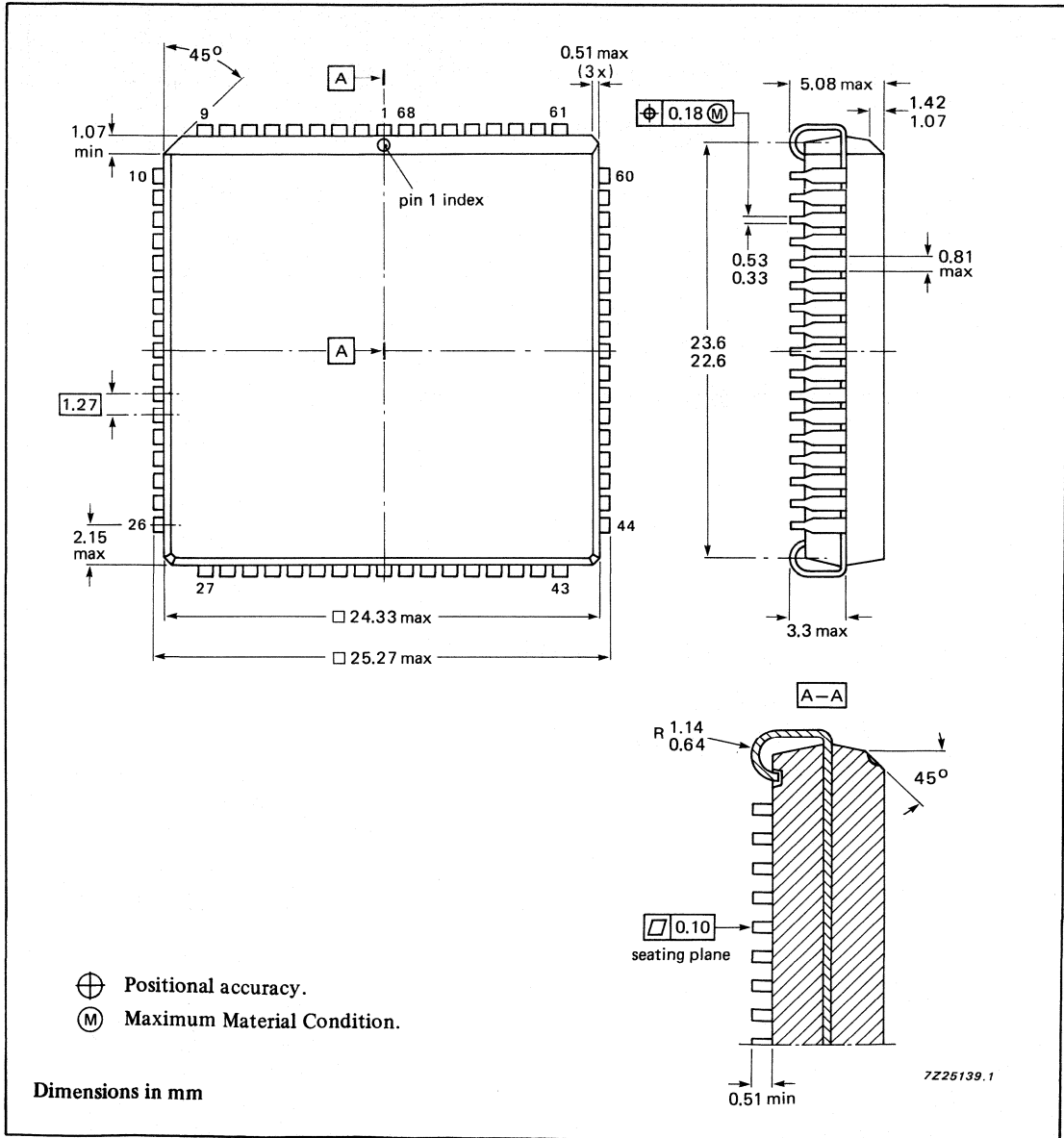
84-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); (SOT189AA, AGA)

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

7Z25140.1
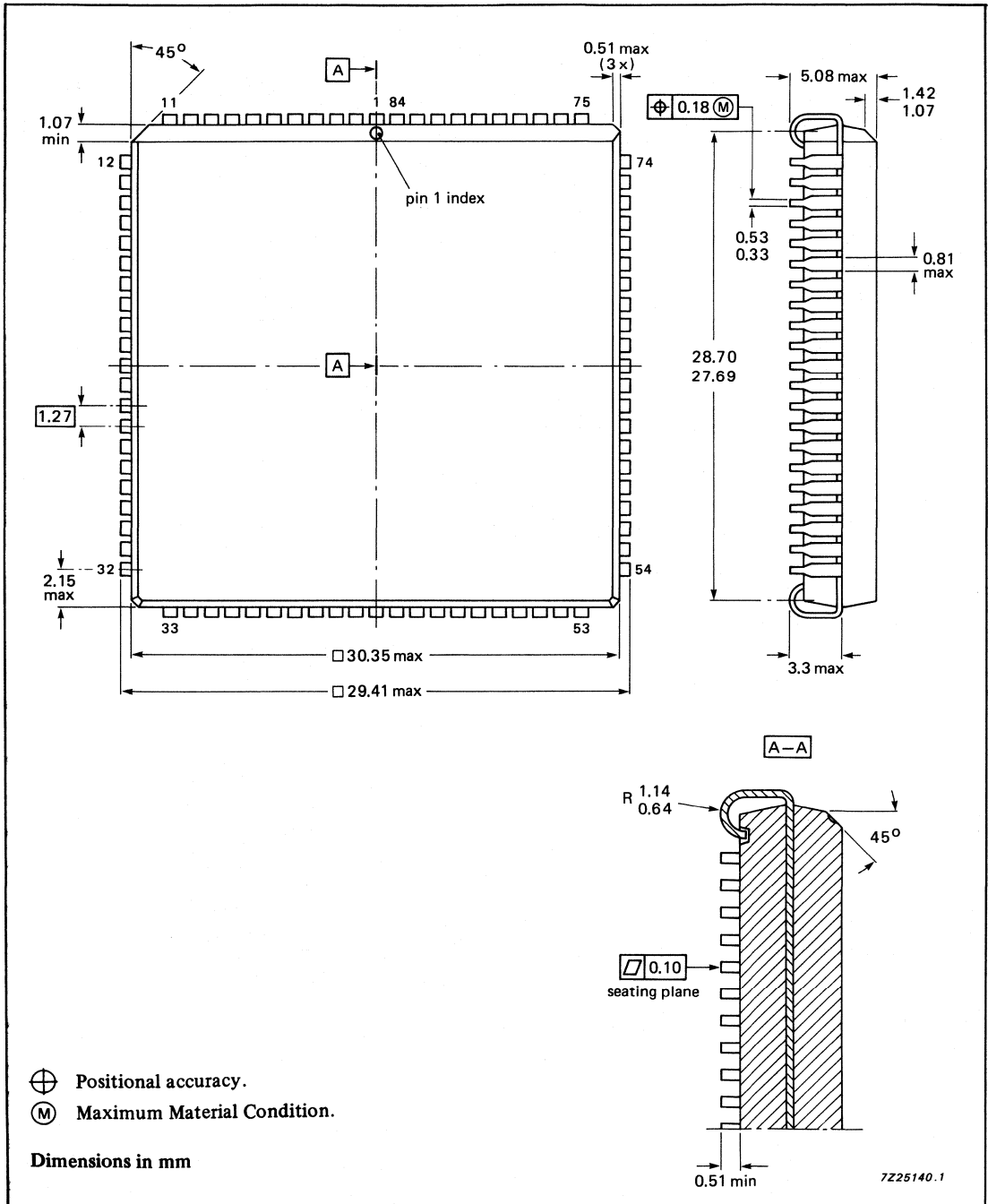
44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205A)

19.2 max

15.9 max

0° min

seating plane

7° max

2.2   2.6 max

0.25
0.14

1.2 min

⬜ 0.2 S

1.05 max   0.25 0.05   S

14   A

B

index corner

44   34

2.8 max

1   pin 1 index

33   2.4 max

14

19.2 max

⊕ 0.1 Ⓜ B

11   23

0.50 0.35

12   22

0.50 0.35   ⊕ 0.1 Ⓜ A   0.56 max

1.0

7Z95754.3

⊕   Positional accuracy.

Ⓜ   Maximum Material Condition.

Dimensions in mm

120-LEAD QUAD FLAT-PACK; PLASTIC (SOT220)

30.6 max

3.35

1.6

seating plane

0.2 S

0.25
0.05

S

33.2 max

0.3 A

3.8 max

0.25
0.14

B

index corner

120

1

pin 1 index

90

91

0.8

28

33.2
max

30.6
max

0.45
0.30

0.1 M

30

61

31

60

28

0.3 B

A

X

7Z30013.1

30.6 max

DETAIL X

0° min

0-7°

1.2

0.5
max

SOLDERING

Plastic mini-packs and plastic leaded chip carriers

By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave) in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

Repairing soldered joints (by hand-held soldering iron or pulse-heated solder tool)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MAGNETIC PRODUCTS*

LIQUID CRYSTAL DISPLAYS

The contents of each series are listed on pages iii to ix.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.

Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

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code	handbook title
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IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom;** Subscriber sets, Cordless Telephones, Mobile/Cellular, Radio Pagers
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; 74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
Supplement **to IC07**	**Advanced CMOS logic (ACL)**
IC08	**10/100K ECL Logic/Memory/PLD**
IC09	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I²C-bus compatible ICs**
IC13	**Programmable Logic Devices (PLD)**
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement **to IC15**	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom;** ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**
IC20	**8051-based 8-bit microcontrollers**
IC23	**Advanced BiCMOS interface logic**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	SC01	Diodes High-voltage tripler units
S2a	SC02	Power diodes
S2b	SC03	Thyristors and triacs
S3	SC04	Small-signal transistors
S4a	SC05	Low-frequency power transistors and hybrid IC power modules
S4b	SC06	High-voltage and switching power transistors
S5	SC07	Small-signal field-effect transistors
S6	SC08a*	RF power bipolar transistors
	SC08b	RF power MOS transistors
	SC09	RF power modules
S7	SC10	Surface mounted semiconductors
S8b	SC12	Optocouplers
S9	SC13*	PowerMOS transistors
S10	SC14	Wideband transistors and wideband hybrid IC modules
S11	SC15	Microwave transistors
S15**	SC16	Laser diodes
S13	SC17	Semiconductor sensors

* Not yet issued with the new code in this series of handbooks.

** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

code	handbook title
DC01	**Colour display components** Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	**Monochrome monitor tubes and deflection units**
DC03	**Television tuners, coaxial aerial input assemblies**
DC04	**Loudspeakers**
DC05	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

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This series of data handbooks comprises:

current code	new code	handbook title
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C11	PA02	Varistors, thermistors and sensors
C12	PA03	Potentiometers and switches
C7	PA04	Variable capacitors
C22	PA05*	Film capacitors
C15	PA06	Ceramic capacitors
C9	PA07*	Piezoelectric quartz devices
C13	PA08	Fixed resistors

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T3	PC01	High-power klystrons and accessories
T5	PC02*	Cathode-ray tubes
T6	PC03*	Geiger-Müller tubes
T9	PC04	Photo multipliers
T10	PC05	Plumbicon camera tubes and accessories
T11	PC06	Circulators and Isolators
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09	Dry-reed switches
	PC11	Solid state image sensors and peripherals integrated circuits
T9	PC12*	Electron multipliers

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current code	new code	handbook title
C4 ⎫ C5 ⎭	MA01	Soft Ferrites
C16	MA02*	Permanent magnet materials
C19	MA03*	Piezoelectric ceramics

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